## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS B200 M6 (Intel Xeon Gold 6336Y, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>343</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>355</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2021  
**Hardware Availability:** Apr-2021  
**Software Availability:** Dec-2020

### Copies

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Base</th>
<th>Peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>96</td>
<td>234</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>96</td>
<td>323</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>96</td>
<td>572</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>96</td>
<td>427</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>96</td>
<td>697</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>96</td>
<td>728</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>96</td>
<td>265</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>96</td>
<td>721</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>96</td>
<td></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>96</td>
<td></td>
</tr>
</tbody>
</table>

### Hardware

**CPU Name:** Intel Xeon Gold 6336Y  
**Max MHz:** 3600  
**Nominal:** 2400  
**Enabled:** 48 cores, 2 chips, 2 threads/core  
**Orderable:** 1.2 Chips  
**Cache L1:** 32 KB I + 48 KB D on chip per core  
**L2:** 1.25 MB I+D on chip per core  
**L3:** 36 MB I+D on chip per chip  
**Other:** None  
**Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R)  
**Storage:** 1 x 480 GB SATA SSD  
**Other:** None

### Software

**OS:** SUSE Linux Enterprise Server 15 SP2  
**Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux  
**Parallel:** No  
**Firmware:** Version 4.2.1c released Jul-2021  
**File System:** btrfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** 32/64-bit  
**Other:** jemalloc memory allocator V5.0.1  
**Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**
Cisco UCS B200 M6 (Intel Xeon Gold 6336Y, 2.40GHz)  

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>96</td>
<td>654</td>
<td>234</td>
<td>654</td>
<td>234</td>
<td>654</td>
<td>234</td>
<td>96</td>
<td>651</td>
<td>272</td>
<td>561</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>96</td>
<td>489</td>
<td>278</td>
<td>490</td>
<td>277</td>
<td>489</td>
<td>278</td>
<td>96</td>
<td>420</td>
<td>323</td>
<td>355</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>96</td>
<td>271</td>
<td>572</td>
<td>272</td>
<td>570</td>
<td>271</td>
<td>573</td>
<td>96</td>
<td>271</td>
<td>572</td>
<td>271</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>96</td>
<td>590</td>
<td>213</td>
<td>591</td>
<td>213</td>
<td>590</td>
<td>213</td>
<td>96</td>
<td>590</td>
<td>213</td>
<td>590</td>
</tr>
<tr>
<td>523.xalanbmk_r</td>
<td>96</td>
<td>237</td>
<td>427</td>
<td>237</td>
<td>428</td>
<td>237</td>
<td>427</td>
<td>96</td>
<td>237</td>
<td>427</td>
<td>237</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>96</td>
<td>242</td>
<td>696</td>
<td>241</td>
<td>697</td>
<td>241</td>
<td>699</td>
<td>96</td>
<td>230</td>
<td>728</td>
<td>231</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>96</td>
<td>416</td>
<td>265</td>
<td>416</td>
<td>264</td>
<td>416</td>
<td>265</td>
<td>96</td>
<td>416</td>
<td>265</td>
<td>416</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>96</td>
<td>612</td>
<td>260</td>
<td>612</td>
<td>260</td>
<td>612</td>
<td>260</td>
<td>96</td>
<td>612</td>
<td>260</td>
<td>612</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>96</td>
<td>349</td>
<td>721</td>
<td>349</td>
<td>721</td>
<td>349</td>
<td>721</td>
<td>96</td>
<td>349</td>
<td>721</td>
<td>349</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>96</td>
<td>538</td>
<td>193</td>
<td>538</td>
<td>193</td>
<td>538</td>
<td>193</td>
<td>96</td>
<td>543</td>
<td>191</td>
<td>544</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base = 343**  
**SPECrate®2017_int_peak = 355**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOC_CONF = "retain:true"
```

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM  
memory using openSUSE Leap 15.2  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6336Y, 2.40GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 343
SPECrate®2017_int_peak = 355

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

General Notes (Continued)

runcpu command invoked through numacll i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acfc64d
running on install Sat Aug 14 18:55:33 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6336Y CPU @ 2.40GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Gold 6336Y, 2.40GHz)

SPECraten®2017_int_base = 343
SPECraten®2017_int_peak = 355

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6336Y CPU @ 2.40GHz
Stepping: 6
CPU MHz: 2468.457
CPU max MHz: 3600.0000
CPU min MHz: 800.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 36864K
NUMA node0 CPU(s): 0-11,48-59
NUMA node1 CPU(s): 12-23,60-71
NUMA node2 CPU(s): 24-35,72-83
NUMA node3 CPU(s): 36-47,84-95
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 fma cx16
xtrunc pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd
mqa ibrs ibpb stibp ibrs_enhanced tpr_shadow vmpress flexpriority ept vpid ept_ad
fssgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni
avx512bw avx512lv xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbb_local wbnoivd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512vbm1 umip pku ospke avx512vbmi2 gfnl vaes vcpulqdq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md_clear pconfig flush_l1d
arch_capabilities

/proc/cpuinfo cache data

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6336Y, 2.40GHz)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6336Y, 2.40GHz)

**SPEC CPU®2017 Integer Rate Result**

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>SPECrate®2017_int_base</td>
<td>343</td>
</tr>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>355</td>
</tr>
</tbody>
</table>

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

---

### Platform Notes (Continued)

Kernel self-reported vulnerability status:

- **CVE-2018-12207 (iTLB Multihit):** Not affected
- **CVE-2018-3620 (L1 Terminal Fault):** Not affected
- **Microarchitectural Data Sampling:** Not affected
- **CVE-2017-5754 (Meltdown):** Not affected
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- **CVE-2020-0543 (Special Register Buffer Data Sampling):** Not affected
- **CVE-2019-11135 (TSX Asynchronous Abort):** Not affected

run-level 3 Aug 14 18:54

SPEC is set to: /home/cpu2017

```
Filesystem  Type     Size  Used Avail Use% Mounted on 
/dev/sda4   btrfs     445G  16G  428G   4% /home
```

From /sys/devices/virtual/dmi/id

<table>
<thead>
<tr>
<th>Vendor:</th>
<th>Cisco Systems Inc</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product:</td>
<td>UCSB-B200-M6</td>
</tr>
<tr>
<td>Serial:</td>
<td>FCH24097576</td>
</tr>
</tbody>
</table>

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:

<table>
<thead>
<tr>
<th>BIOS Vendor:</th>
<th>Cisco Systems, Inc.</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIOS Version:</td>
<td>B200M6.4.2.1c.10.0723211453</td>
</tr>
<tr>
<td>BIOS Date:</td>
<td>07/23/2021</td>
</tr>
<tr>
<td>BIOS Revision:</td>
<td>5.22</td>
</tr>
</tbody>
</table>

(End of data from sysinfo program)
## Compiler Version Notes

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r (peak) 557.xz_r (peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) C</td>
<td>Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000</td>
</tr>
<tr>
<td>Copyright (C)</td>
<td>1985-2020 Intel Corporation. All rights reserved.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>C</th>
<th>502.gcc_r (peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C)</td>
<td>1985-2020 Intel Corporation. All rights reserved.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r (base) 502.gcc_r (base) 505.mcf_r (base, peak) 525.x264_r (base, peak) 557.xz_r (base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C)</td>
<td>1985-2020 Intel Corporation. All rights reserved.</td>
</tr>
</tbody>
</table>

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6336Y, 2.40GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

Compiler Version Notes (Continued)

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
| C       | 500.perlbench_r(peak) 557.xz_r(peak) |
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

------------------------------------------------------------------------------
| C       | 502.gcc_r(peak) |
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

------------------------------------------------------------------------------
| C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base) |
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

------------------------------------------------------------------------------
| C++      | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak) |
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

------------------------------------------------------------------------------
| Fortran  | 548.exchange2_r(base, peak) |
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6336Y, 2.40GHz)

| Copyright 2017-2021 Standard Performance Evaluation Corporation |

SPECrater®2017_int_base = 343
SPECrater®2017_int_peak = 355

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

**Base Compiler Invocation**

C benchmarks:
- icx

C++ benchmarks:
- icpx

Fortran benchmarks:
- ifort

**Base Portability Flags**

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

(Continued on next page)
### Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6336Y, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 343</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak = 355</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Aug-2021

**Hardware Availability:** Apr-2021

**Software Availability:** Dec-2020

### Base Optimization Flags (Continued)

Fortran benchmarks (continued):
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

### Peak Compiler Invocation

C benchmarks (except as noted below):
- `icx`
- `500.perlbench_r: icc`
- `557.xz_r: icc`

C++ benchmarks:
- `icpx`

Fortran benchmarks:
- `ifort`

### Peak Portability Flags

- `500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64`
- `502.gcc_r: -D_FILE_OFFSET_BITS=64`
- `505.mcf_r: -DSPEC_LP64`
- `520.omnetpp_r: -DSPEC_LP64`
- `523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX`
- `525.x264_r: -DSPEC_LP64`
- `531.deepsjeng_r: -DSPEC_LP64`
- `541.leela_r: -DSPEC_LP64`
- `548.exchange2_r: -DSPEC_LP64`
- `557.xz_r: -DSPEC_LP64`

### Peak Optimization Flags

C benchmarks:
- `500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-mem-layout-trans=4 -fno-strict-overflow -mbranches-within-32B-boundaries`

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6336Y, 2.40GHz)

**SPEC CPU®2017 Integer Rate Result**

**SPECrate®2017_int_base = 343**

**SPECrate®2017_int_peak = 355**

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

**Peak Optimization Flags (Continued)**

500.perlbench_r (continued):
-`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
-`-lqkmalloc`

502.gcc_r: `-m32`
-`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin`
-`-std=gnu89`
-`-Wl,-z,muldefs -fprofile-generate(pass1)`
-`-fprofile-use=default.profdata(pass2) -xCORE-AVX512 -flto`
-`-Ofast(pass1) -O3 -ffast-math -qopt-mem-layout-trans=4`
-`-mbranches-within-32B-boundaries`
-`-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc`

505.mcf_r: `basepeak = yes`

525.x264_r: `--w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto`
-`-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias`
-`-mbranches-within-32B-boundaries`
-`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
-`-lqkmalloc`

557.xz_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
-`-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries`
-`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
-`-lqkmalloc`

C++ benchmarks:

520.omnetpp_r: `basepeak = yes`

523.xalancbmk_r: `basepeak = yes`

531.deepsjeng_r: `basepeak = yes`

541.leela_r: `basepeak = yes`

Fortran benchmarks:

548.exchange2_r: `basepeak = yes`

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6336Y, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 343</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak = 355</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Aug-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2021</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Dec-2020</td>
</tr>
</tbody>
</table>

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.