Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>326</td>
<td>330</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Aug-2021  
Hardware Availability: Apr-2021

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base (326)</th>
<th>SPECrate®2017_fp_peak (330)</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r 96</td>
<td></td>
</tr>
<tr>
<td>507.cactuBSSN_r 96</td>
<td></td>
</tr>
<tr>
<td>508.namd_r 96</td>
<td></td>
</tr>
<tr>
<td>510.parest_r 96</td>
<td></td>
</tr>
<tr>
<td>511.povray_r 96</td>
<td></td>
</tr>
<tr>
<td>519.lbm_r 96</td>
<td></td>
</tr>
<tr>
<td>521.wrf_r 96</td>
<td></td>
</tr>
<tr>
<td>526.blender_r 96</td>
<td></td>
</tr>
<tr>
<td>527.cam4_r 96</td>
<td></td>
</tr>
<tr>
<td>538.imagick_r 96</td>
<td></td>
</tr>
<tr>
<td>544.nab_r 96</td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r 96</td>
<td></td>
</tr>
<tr>
<td>554.roms_r 96</td>
<td></td>
</tr>
</tbody>
</table>

**Hardware**  
CPU Name: Intel Xeon Gold 5318S  
Max MHz: 3400  
Nominal: 2100  
Enabled: 48 cores, 2 chips, 2 threads/core  
Orderable: 1,2 Chips  
Cache L1: 32 KB I + 48 KB D on chip per core  
L2: 1.25 MB I+D on chip per core  
L3: 36 MB I+D on chip per chip  
Other: None  
Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2933)  
Storage: 1 x 300 GB 15K SAS HDD  
Other: None

**Software**  
OS: SUSE Linux Enterprise Server 15 SP2  
5.3.18-22-default  
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;  
Classic Build 20201112 for Linux  
Parallel: No  
Firmware: Version 4.2.1c released Jul-2021  
File System: btrfs  
System State: Run level 3 (multi-user)  
Base Pointers: 64-bit  
Peak Pointers: 64-bit  
Other: jemalloc memory allocator V5.0.1  
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems  
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Aug-2021  
Hardware Availability: Apr-2021  
Software Availability: Dec-2020

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>96</td>
<td>1467</td>
<td>656</td>
<td>1467</td>
<td>656</td>
<td>1468</td>
<td>656</td>
<td>96</td>
<td>1470</td>
<td>655</td>
<td>1468</td>
<td>656</td>
<td>96</td>
<td>1468</td>
<td>656</td>
<td></td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>96</td>
<td>269</td>
<td>451</td>
<td>269</td>
<td>452</td>
<td>269</td>
<td>451</td>
<td>96</td>
<td>269</td>
<td>451</td>
<td>269</td>
<td>452</td>
<td>269</td>
<td>452</td>
<td>269</td>
<td>451</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>96</td>
<td>390</td>
<td>234</td>
<td>390</td>
<td>234</td>
<td>390</td>
<td>234</td>
<td>96</td>
<td>390</td>
<td>234</td>
<td>390</td>
<td>234</td>
<td>390</td>
<td>234</td>
<td>390</td>
<td>234</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>96</td>
<td>1404</td>
<td>179</td>
<td>1399</td>
<td>179</td>
<td>1400</td>
<td>179</td>
<td>96</td>
<td>1397</td>
<td>180</td>
<td>1397</td>
<td>180</td>
<td>1395</td>
<td>180</td>
<td>1395</td>
<td>180</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>96</td>
<td>632</td>
<td>355</td>
<td>634</td>
<td>354</td>
<td>631</td>
<td>355</td>
<td>96</td>
<td>550</td>
<td>408</td>
<td>550</td>
<td>408</td>
<td>547</td>
<td>409</td>
<td>547</td>
<td>409</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>96</td>
<td>418</td>
<td>242</td>
<td>419</td>
<td>242</td>
<td>418</td>
<td>242</td>
<td>96</td>
<td>418</td>
<td>242</td>
<td>419</td>
<td>242</td>
<td>418</td>
<td>242</td>
<td>418</td>
<td>242</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>96</td>
<td>709</td>
<td>303</td>
<td>703</td>
<td>306</td>
<td>727</td>
<td>296</td>
<td>96</td>
<td>716</td>
<td>300</td>
<td>715</td>
<td>301</td>
<td>714</td>
<td>301</td>
<td>714</td>
<td>301</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>96</td>
<td>484</td>
<td>347</td>
<td>488</td>
<td>344</td>
<td>486</td>
<td>346</td>
<td>96</td>
<td>484</td>
<td>347</td>
<td>488</td>
<td>344</td>
<td>486</td>
<td>346</td>
<td>486</td>
<td>346</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>96</td>
<td>294</td>
<td>813</td>
<td>290</td>
<td>823</td>
<td>288</td>
<td>829</td>
<td>96</td>
<td>294</td>
<td>813</td>
<td>290</td>
<td>823</td>
<td>288</td>
<td>829</td>
<td>288</td>
<td>829</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>96</td>
<td>300</td>
<td>538</td>
<td>300</td>
<td>538</td>
<td>298</td>
<td>543</td>
<td>96</td>
<td>294</td>
<td>549</td>
<td>295</td>
<td>548</td>
<td>295</td>
<td>548</td>
<td>295</td>
<td>548</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>96</td>
<td>1815</td>
<td>206</td>
<td>1814</td>
<td>206</td>
<td>1814</td>
<td>206</td>
<td>96</td>
<td>1815</td>
<td>206</td>
<td>1814</td>
<td>206</td>
<td>1814</td>
<td>206</td>
<td>1814</td>
<td>206</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>96</td>
<td>1101</td>
<td>139</td>
<td>1099</td>
<td>139</td>
<td>1095</td>
<td>139</td>
<td>96</td>
<td>1092</td>
<td>140</td>
<td>1102</td>
<td>138</td>
<td>1101</td>
<td>139</td>
<td>1101</td>
<td>139</td>
</tr>
</tbody>
</table>

SPECrate\textsuperscript{2017}_fp_base = 326
SPECrate\textsuperscript{2017}_fp_peak = 330

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

SPECrate®2017_fp_base = 326
SPECrate®2017_fp_peak = 330

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numaclt i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on localhost Fri Aug 13 05:21:21 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5318S CPU @ 2.10GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
Platform Notes (Continued)

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 5318S CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2626.997
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 36864K
NUMA node0 CPU(s): 0-11,48-59
NUMA node1 CPU(s): 12-23,60-71
NUMA node2 CPU(s): 24-35,72-83
NUMA node3 CPU(s): 36-47,84-95
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcpid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsavec xgetbv1 xsavevs cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local wbnoinzvd dtether ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vmbi umip pkp ospke avx512_vmbi2 gfnf vaes vpcmldqd avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_lid arch_capabilities

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

Platform Notes (Continued)

/platform/cpuinfo cache data
  cache size : 36864 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 48 49 50 51 52 53 54 55 56 57 58 59
  node 0 size: 257635 MB
  node 0 free: 244029 MB
  node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 60 61 62 63 64 65 66 67 68 69 70 71
  node 1 size: 258042 MB
  node 1 free: 247656 MB
  node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 72 73 74 75 76 77 78 79 80 81 82 83
  node 2 size: 258042 MB
  node 2 free: 248054 MB
  node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 84 85 86 87 88 89 90 91 92 93 94 95
  node 3 size: 258005 MB
  node 3 free: 248108 MB
  node distances:
    node  0   1   2   3
    0:  10  11  20  20
    1:  11  10  20  20
    2:  20  20  10  11
    3:  20  20  11  10

From /proc/meminfo
  MemTotal: 1056486416 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu/*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

  uname -a:
    Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
    x86_64 x86_64 GNU/Linux

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 326
SPECrate®2017_fp_peak = 330

Copyright 2017-2021 Standard Performance Evaluation Corporation

Platform Notes (Continued)

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapgs barriers and __user pointer sanitation
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitation
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Aug 12 21:21

SPEC is set to: /home/cpu2017
FileSystem     Type   Size   Used  Avail  Use% Mounted on
/dev/sda2       btrfs   222G   70G  151G  32%    /home

From /sys/devices/virtual/dmi/id
Vendor:    Cisco Systems Inc
Product:   UCSC-C220-M6S
Serial:    WZP24430ADF

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2933

BIOS:
BIOS Vendor:     Cisco Systems, Inc.
BIOS Version:    C220M6.4.2.1c.1.0701210708
BIOS Date:       07/01/2021
BIOS Revision:   5.22

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

SPECrater®2017_fp_base = 326
SPECrater®2017_fp_peak = 330

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,</td>
<td></td>
</tr>
<tr>
<td>Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>C++</td>
<td>508.namd_r(base, peak) 510.parest_r(base, peak)</td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,</td>
<td></td>
</tr>
<tr>
<td>Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>C++, C</td>
<td>511.povray_r(peak)</td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on</td>
<td></td>
</tr>
<tr>
<td>Intel(R) 64, Version 2021.1 Build 20201112_000000</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)</td>
<td></td>
</tr>
<tr>
<td>64, Version 2021.1 Build 20201112_000000</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>C++, C</td>
<td>511.povray_r(base) 526.blender_r(base, peak)</td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,</td>
<td></td>
</tr>
<tr>
<td>Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,</td>
<td></td>
</tr>
<tr>
<td>Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>C++, C</td>
<td>511.povray_r(peak)</td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on</td>
<td></td>
</tr>
<tr>
<td>Intel(R) 64, Version 2021.1 Build 20201112_000000</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)</td>
<td></td>
</tr>
<tr>
<td>64, Version 2021.1 Build 20201112_000000</td>
<td></td>
</tr>
</tbody>
</table>
| (Continued on next page)
Cisco Systems  
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base = 326**

**SPECrate®2017_fp_peak = 330**

---

## Compiler Version Notes (Continued)

---

C++, C  
| 511.povray_r(base) 526.blender_r(base, peak)  
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
---

C++, C, Fortran  
| 507.cactuBSSN_r(base, peak)  
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
---

Fortran  
| 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)  
| 554.roms_r(base, peak)  
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
---

Fortran, C  
| 521.wrf_r(peak)  
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
---

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>326</td>
<td>330</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

---

Compiler Version Notes (Continued)

Fortran, C      | 521.wrf_r(base) 527.cam4_r(base, peak)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

Fortran, C      | 521.wrf_r(peak)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

Fortran, C      | 521.wrf_r(base) 527.cam4_r(base, peak)
-------------------------------------------------------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-------------------------------------------------------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)  

SPECrate®2017_fp_base = 326  
SPECrate®2017_fp_peak = 330

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

Test Date: Aug-2021  
Hardware Availability: Apr-2021  
Software Availability: Dec-2020

**Base Compiler Invocation (Continued)**

Benchmarks using both Fortran and C:  
ifort icx

Benchmarks using both C and C++:  
icpx icx

Benchmarks using Fortran, C, and C++:  
icpx icx ifort

**Base Portability Flags**

503.bwaves_r: -DSPEC_LP64  
507.cactuBSSN_r: -DSPEC_LP64  
508.namd_r: -DSPEC_LP64  
510.parest_r: -DSPEC_LP64  
511.povray_r: -DSPEC_LP64  
519.lbm_r: -DSPEC_LP64  
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian  
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char  
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG  
538.imagick_r: -DSPEC_LP64  
544.nab_r: -DSPEC_LP64  
549.fotonik3d_r: -DSPEC_LP64  
554.roms_r: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:  
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math  
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4  
-mbranches-within-32B-boundaries -ljemalloc  
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:  
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto  
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4  
-mbranches-within-32B-boundaries -ljemalloc  
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:  
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div  
-qopt-prefetch -ffinite-math-only

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

| CPU2017 License: 9019 | Test Date: Aug-2021 |
| Test Sponsor: Cisco Systems | Hardware Availability: Apr-2021 |
| Tested by: Cisco Systems | Software Availability: Dec-2020 |

**Base Optimization Flags (Continued)**

Fortran benchmarks (continued):
- `-qopt-multiple-gather-scatter-by-shuffles` `-qopt-mem-layout-trans=4`
- `-nostandard-realloc-lhs` `-align array32byte` `-auto`
- `-mbranches-within-32B-boundaries` `-ljemalloc`
- `-L/usr/local/jemalloc64-5.0.1/lib`

Benchmarks using both Fortran and C:
- `-w` `-m64` `-std=c11` `-Wl,-z,muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math`
- `-flto` `-mfpmath=sse` `-funroll-loops` `-qopt-mem-layout-trans=4` `-O3` `-ipo`
- `-no-prec-div` `-qopt-prefetch` `-ffinite-math-only`
- `-qopt-multiple-gather-scatter-by-shuffles`
- `-mbranches-within-32B-boundaries` `-nostandard-realloc-lhs`
- `-align array32byte` `-auto` `-ljemalloc` `-L/usr/local/jemalloc64-5.0.1/lib`

Benchmarks using both C and C++:
- `-w` `-m64` `-std=c11` `-Wl,-z,muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math`
- `-flto` `-mfpmath=sse` `-funroll-loops` `-qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries` `-ljemalloc`
- `-L/usr/local/jemalloc64-5.0.1/lib`

Benchmarks using Fortran, C, and C++:
- `-w` `-m64` `-std=c11` `-Wl,-z,muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math`
- `-flto` `-mfpmath=sse` `-funroll-loops` `-qopt-mem-layout-trans=4` `-O3`
- `-no-prec-div` `-qopt-prefetch` `-ffinite-math-only`
- `-qopt-multiple-gather-scatter-by-shuffles`
- `-mbranches-within-32B-boundaries` `-nostandard-realloc-lhs`
- `-align array32byte` `-auto` `-ljemalloc` `-L/usr/local/jemalloc64-5.0.1/lib`

**Peak Compiler Invocation**

C benchmarks:
- `icx`

C++ benchmarks:
- `icpx`

Fortran benchmarks:
- `ifort`

Benchmarks using both Fortran and C:
- `521.wrf_r:ifort icc`

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

SPECrate®2017_fp_base = 326
SPECrate®2017_fp_peak = 330

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Peak Compiler Invocation (Continued)

527.cam4_r: ifort icx

Benchmarks using both C and C++:
511.povray_r: icpc icc
526.blender_r: icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-Ofast -qopt-mem-layout-trans=4 -fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
508.namd_r: basepeak = yes
510.parest_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
503.bwaves_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -03 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

SPECrate®2017_fp_base = 326
SPECrate®2017_fp_peak = 330

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Peak Optimization Flags (Continued)

503.bwaves_r (continued):
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

549.fotonik3d_r: basepeak = yes
554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
## Cisco Systems

Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 326</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = 330</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Aug-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2021</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Dec-2020</td>
</tr>
</tbody>
</table>

---

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-08-13 05:21:20-0400.
Report generated on 2021-09-01 14:26:29 by CPU2017 PDF formatter v6442.
Originally published on 2021-08-31.