### SPEC CPU®2017 Integer Rate Result

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)

**Tyrone Camarero DIT400TR-28R**  
(2.10 GHz, Intel Xeon Gold 5218R)

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- **CPU2017 License**: 006042  
- **Test Sponsor**: Netweb Pte Ltd  
- **Tested by**: Tyrone Systems  
- **Test Date**: Jul-2021  
- **Hardware Availability**: Feb-2020  
- **Software Availability**: Jun-2021

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<table>
<thead>
<tr>
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<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
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<tr>
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<td>xz_r</td>
<td>80</td>
<td>146</td>
<td>535</td>
</tr>
</tbody>
</table>

---

#### Hardware

- **CPU Name**: Intel Xeon Gold 5218R  
- **Max MHz**: 4000  
- **Nominal**: 2100  
- **Enabled**: 40 cores, 2 chips, 2 threads/core  
- **Orderable**: 1.2 Chips  
- **Cache L1**: 32 KB I + 32 KB D on chip per core  
- **L2**: 1 MB I+D on chip per core  
- **L3**: 27.5 MB I+D on chip per chip  
- **Other**: None  
- **Memory**: 384 GB (12 x 32 GB 2Rx4 PC4-2933P-R, running at 2666)  
- **Storage**: 1 x 480 GB SATA SSD  
- **Other**: None

---

#### Software

- **OS**: CentOS Linux release 8.4.2105  
  Kernel 4.18.0-305.3.1.el8.x86_64  
- **Compiler**: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++  
  Compiler Build 20201113 for Linux;  
  Fortran: Version 2021.1 of Intel Fortran Compiler  
  Classic Build 20201112 for Linux;  
  C/C++: Version 2021.1 of Intel C/C++ Compiler  
  Classic Build 20201112 for Linux
- **Parallel**: No  
- **Firmware**: Version 3.4a released Jan-2021  
- **File System**: xfs  
- **System State**: Run level 3 (multi-user)  
- **Base Pointers**: 64-bit  
- **Peak Pointers**: 32/64-bit  
- **Other**: Jemalloc memory allocator V5.0.1  
- **Power Management**: BIOS set to prefer performance at the cost of additional power usage.
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SPECrate®2017_int_base = 242
SPECrate®2017_int_peak = 251

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
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<th>Seconds</th>
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<td>146</td>
<td>593</td>
<td>146</td>
<td>593</td>
<td>146</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOCONF = "retain:true"

General Notes

Binaries compiled locally by Netweb
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

(Continued on next page)
**General Notes (Continued)**

`numactl --interleave=all runcpu <etc>`

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.


**Platform Notes**

BIOS Settings:
Power Technology set to Custom
Power Performance Tuning set to BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode set to Performance
LLC Dead Line Alloc set to Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca64d running on localhost.localdomain Tue Jul 27 12:33:38 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
  2  "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu from util-linux 2.32.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2

(Continued on next page)
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SPECrate®2017_int_base = 242
SPECrate®2017_int_peak = 251

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Platform Notes (Continued)

Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
BIOS Vendor ID: Intel(R) Corporation
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
BIOS Model name: Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
Stepping: 7
CPU MHz: 2899.589
CPU max MHz: 4000.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-19,40-59
NUMA node1 CPU(s): 20-39,60-79

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aerfperforf pni pclmulqdq dtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm
pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c
rdread rdwrand lahflm abm 3nowprefetch cpuid_fault eplt cdp _13 invpcid_single
intel_pni ssbd mba ibbp stibp ibrs enabled tpr_shadow vmx flexpriority ept
vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cmx mxrt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves cmq llc cmq_occup llc cmq_mbm_total cmq_mbm_local
dtherm ida arat pln pts pkup ospte avx512_vnni md_clear flush_l1d arch_capabilities

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55 56 57 58 59
node 0 size: 192115 MB
node 0 free: 178593 MB
node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 60 61 62 63 64
65 66 67 68 69 70 71 72 73 74 75 76 77 78 79
node 1 size: 193489 MB
node 1 free: 184955 MB

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

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CPU2017 License: 006042
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Tested by: Tyrone Systems

Test Date: Jul-2021
Hardware Availability: Feb-2020
Software Availability: Jun-2021

Platform Notes (Continued)

node distances:
node  0  1
  0:  10  21
  1:  21  10

From /proc/meminfo
MemTotal:       394859744 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sbin/tuned-adm active
  Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
  performance

From /etc/*release* /etc/*version*
centos-release: CentOS Linux release 8.4.2105
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.4
os-release:
  NAME="CentOS Linux"
  VERSION="8"
  ID="centos"
  ID_LIKE="rhel fedora"
  VERSION_ID="8"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="CentOS Linux 8"
  ANSI_COLOR="0;31"
redhat-release: CentOS Linux release 8.4.2105
system-release: CentOS Linux release 8.4.2105
system-release-cpe: cpe:/o:centos:centos:8

uname -a:
  Linux localhost.localdomain 4.18.0-305.3.1.el8.x86_64 #1 SMP Tue Jun 1 16:14:33 UTC 2021 x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):
  KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault):
  Not affected
Microarchitectural Data Sampling:
  Not affected
CVE-2017-5754 (Meltdown):
  Not affected
CVE-2018-3639 (Speculative Store Bypass):
  Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):
  Mitigation: usercopy/swaps barriers and __user pointer

(Continued on next page)
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**Platform Notes (Continued)**

CPE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CPE-2020-0543 (Special Register Buffer Data Sampling):
Not affected

CPE-2019-11135 (TSX Asynchronous Abort):
Mitigation: TSX disabled

run-level 3 Jul 27 05:52

SPEC is set to: /home/cpu2017

Filesystem          Type  Size  Used Avail Use% Mounted on
/dev/mapper/cl-home xfs   372G  5.8G  366G   2% /home

From /sys/devices/virtual/dmi/id
Vendor:         Tyrone Systems
Product:        Tyrone Camarero DS400TR-28R
Serial:         0123456789

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

BIOS:
BIOS Vendor:       American Megatrends Inc.
BIOS Version:      3.4a
BIOS Date:         01/07/2021
BIOS Revision:     5.14

(End of data from sysinfo program)

**Compiler Version Notes**

==============================================================================
C       | 500.perlbench_r(peak) 557.xz_r(peak)
-----------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
   64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

==============================================================================
C       | 502.gcc_r(peak)
-----------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version

(Continued on next page)
**SPEC CPU®2017 Integer Rate Result**

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### Compiler Version Notes (Continued)

2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)  
   525.x264_r(base, peak) 557.xz_r(base)
```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
C | 500.perlbench_r(peak) 557.xz_r(peak)
```

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64,  
Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
C | 502.gcc_r(peak)
```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version  
2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)  
   525.x264_r(base, peak) 557.xz_r(base)
```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
C | 500.perlbench_r(peak) 557.xz_r(peak)
```

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64,  
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Compiler Version Notes (Continued)

C                  | 502.gcc_r(peak)
-------------------|-------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C                  | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base)
-------------------|---------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++                 | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
---------------------|-------------------------------------------------------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran            | 548.exchange2_r(base, peak)
-------------------|------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx
C++ benchmarks:
icpx
Fortran benchmarks:
ifort
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### Base Portability Flags

- 500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
- 502.gcc_r: `-DSPEC_LP64`
- 505.mcf_r: `-DSPEC_LP64`
- 520.omnetpp_r: `-DSPEC_LP64`
- 523.xalancbmk_r: `-DSPEC_LP64 -DSPEC_LINUX`
- 525.x264_r: `-DSPEC_LP64`
- 531.deepsjeng_r: `-DSPEC_LP64`
- 541.leela_r: `-DSPEC_LP64`
- 548.exchange2_r: `-DSPEC_LP64`
- 557.xz_r: `-DSPEC_LP64`

### Base Optimization Flags

**C benchmarks:**

- `-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math`
- `-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries`
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

**C++ benchmarks:**

- `-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto`
- `-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries`
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

**Fortran benchmarks:**

- `-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div`
- `-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`
- `-auto -mbranches-within-32B-boundaries`
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

---

### Peak Compiler Invocation

**C benchmarks (except as noted below):**

- `icx`

- `500.perlbench_r: icc`

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DIT400TR-28R
(2.10 GHz, Intel Xeon Gold 5218R)

SPECrate®2017_int_base = 242
SPECrate®2017_int_peak = 251

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Jul-2021
Hardware Availability: Feb-2020
Software Availability: Jun-2021

Peak Compiler Invocation (Continued)

557.xz_r: icc
C++ benchmarks:
icpx
Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64 -DSPEC_LINUX
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -03 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -fto
-ofast(pass 1) -03 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: basepeak = yes

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

### Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

<table>
<thead>
<tr>
<th>CPU2017 License</th>
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### Tyrone Camarero DIT400TR-28R
(2.10 GHz, Intel Xeon Gold 5218R)

<table>
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</thead>
<tbody>
<tr>
<td>242</td>
<td>251</td>
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</tbody>
</table>

### Peak Optimization Flags (Continued)

525.x264_r:  
- w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto  
-03 -ffast-math -qopt-mem-layout-trans=4 -fno-alias  
-mbranches-within-32B-boundaries  
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin  
-1qkmalloc

557.xz_r:  
- Wl,-z,muldefs -xCORE-AVX512 -ipo -03 -no-prec-div  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin  
-1qkmalloc

C++ benchmarks:

520.omnetpp_r:  
basepeak = yes

523.xalancbmk_r:  
basepeak = yes

531.deepsjeng_r:  
basepeak = yes

541.leela_r:  
basepeak = yes

Fortran benchmarks:

548.exchange2_r:  
basepeak = yes

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-07-27 12:33:37-0400.
Report generated on 2021-09-21 16:16:11 by CPU2017 PDF formatter v6442.
Originally published on 2021-09-21.