## SPEC CPU®2017 Integer Rate Result

**SPEC CPU®2017 int_base = 188**  
**SPEC CPU®2017 int_peak = 194**

<table>
<thead>
<tr>
<th>Program</th>
<th>Copies</th>
<th>SPECrate®2017_int_base (188)</th>
<th>SPECrate®2017_int_peak (194)</th>
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<tr>
<td>500.perlbench_r</td>
<td>64</td>
<td>148</td>
<td>313</td>
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<tr>
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<tr>
<td>557.xz_r</td>
<td>64</td>
<td>115</td>
<td>372</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Silver 4216  
- **Max MHz:** 3200  
- **Nominal:** 2100  
- **Enabled:** 32 cores, 2 chips, 2 threads/core  
- **Orderable:** 1,2 Chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 22 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933P-R, running at 2400)  
- **Storage:** 1 x 480 GB SATA SSD  
- **Other:** None

### Software

- **OS:** CentOS Linux release 8.4.2105  
- **Kernel:** 4.18.0-305.3.1.el8.x86_64  
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
- **Parallel:** No  
- **Firmware:** Version V8.104 released Jul-2021  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage.
### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>115</td>
<td>600</td>
<td>115</td>
<td>601</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

`LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOC_CONF = "retain:true"

(Continued on next page)
Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DIT400TR-48RL
(2.10 GHz, Intel Xeon Silver 4216)

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

SPECrate®2017_int_base = 188
SPECrate®2017_int_peak = 194

Test Date: Aug-2021
Hardware Availability: Apr-2019
Software Availability: Jul-2021

General Notes (Continued)

numactl --interleave=all runcpu <etc>

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Power Technology set to Custom
Power Performance Tuning set to BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode set to Performance
LLC Dead Line Alloc set to Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aaca64d
running on localhost.localdomain Fri Aug  6 11:57:26 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
  2 "physical id"s (chips)
  64 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 16
    siblings : 32
    physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
    physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu from util-linux 2.32.1:
  Architecture:       x86_64
  CPU op-mode(s):    32-bit, 64-bit
  Byte Order:        Little Endian
  CPU(s):            64
  On-line CPU(s) list: 0-63
  Thread(s) per core:  2

(Continued on next page)
Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DIT400TR-48RL
(2.10 GHz, Intel Xeon Silver 4216)

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

SPEC CPU®2017 Integer Rate Result

SPECrate®2017_int_base = 188
SPECrate®2017_int_peak = 194

Platform Notes (Continued)

Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
BIOS Vendor ID: Intel(R) Corporation
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
BIOS Model name: Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
Stepping: 7
CPU MHz: 800.060
CPU max MHz: 3200.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-15,32-47
NUMA node1 CPU(s): 16-23,48-63

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperf perf inspected pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xptr pdcm pcd dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cd8 c8
invpcid_single intel_puin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmni
flexpriority ept vpid etp_ad fsbgbase tsc_adjust bmi1 hle avx2 smep bmi2 erms
invpcid crmq mxr dtr_a avx512f avx512dq rdseed adx smap clfushopt clwb intel_pt
avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves crmq_llc crqm_occup_llc
crqm_mbb_total crqm_mbb_local dtm epi arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req pkpu ospke avx512_vnni md_clear flush_l1d arch_capabilities

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 32 33 34 35 36 37 38 39 40 41 42 43
44 45 46 47
node 0 size: 192106 MB
node 0 free: 191372 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 48 49 50 51 52 53 54 55 56
57 58 59 60 61 62 63
node 1 size: 193491 MB

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DIT400TR-48RL
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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

SPECrate®2017_int_base = 188
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Tyrone Systems
(Continued on next page)

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Test Date: Aug-2021
Hardware Availability: Apr-2019
Software Availability: Jul-2021

Platform Notes (Continued)

node 1 free: 192942 MB
node distances:
node 0 1
 0: 10 21
 1: 21 10

From /proc/meminfo
MemTotal: 394851992 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sbin/tuned-adm active
  Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
  centos-release: CentOS Linux release 8.4.2105
  centos-release-upstream: Derived from Red Hat Enterprise Linux 8.4
  os-release:
    NAME="CentOS Linux"
    VERSION="8"
    ID="centos"
    ID_LIKE="rhel fedora"
    VERSION_ID="8"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="CentOS Linux 8"
    ANSI_COLOR="0;31"
  redhat-release: CentOS Linux release 8.4.2105
  system-release: CentOS Linux release 8.4.2105
  system-release-cpe: cpe:/o:centos:centos:8

uname -a:
  Linux localhost.localdomain 4.18.0-305.3.1.el8.x86_64 #1 SMP Tue Jun 1 16:14:33 UTC 2021 x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): KVM: Mitigation: Split huge pages Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling:
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs

(Continued on next page)
Platform Notes (Continued)

barriers and __user pointer sanitization
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
Mitigation: TSX disabled

run-level 3 Aug 6 11:27

SPEC is set to: /home/cpu2017
Filesystem          Type  Size  Used Avail Use% Mounted on
/dev/mapper/cl-home xfs   372G   76G  296G  21% /home

From /sys/devices/virtual/dmi/id
Vendor:         Tyrone Systems
Product:        Tyrone Camarero DIT400TR-48RL
Product Family: empty
Serial:         empty

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

BIOS:
BIOS Vendor:       American Megatrends Inc.
BIOS Version:      V8.104
BIOS Date:         07/27/2021
BIOS Revision:     5.14
Firmware Revision: 6.1

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r(peak) 557.xz_r(peak)</th>
</tr>
</thead>
</table>
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero DIT400TR-48RL  
(2.10 GHz, Intel Xeon Silver 4216)

<table>
<thead>
<tr>
<th>CPU2017 License: 006042</th>
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<tr>
<td>Test Sponsor: Netweb Pte Ltd</td>
<td>Hardware Availability: Apr-2019</td>
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<tr>
<td>Tested by: Tyrone Systems</td>
<td>Software Availability: Jul-2021</td>
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### Compiler Version Notes (Continued)

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Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113  
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==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)  
455.x264_r(base, peak) 557.xz_r(base)  
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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C       | 500.perlbench_r(peak) 502.gcc_r(base) 505.mcf_r(base, peak)  
455.x264_r(base, peak) 557.xz_r(base)  
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
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C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)  
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
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Tyrone Systems  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero DIT400TR-48RL  
(2.10 GHz, Intel Xeon Silver 4216)  

SPEC CPU®2017 Integer Rate Result  

SPECrater®2017_int_base = 188  
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Compiler Version Notes (Continued)

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Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version  
2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
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C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)  
| 525.x264_r(base, peak) 557.xz_r(base)
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

------------------------------------------------------------------------------
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)  
| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

------------------------------------------------------------------------------
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:  
icx

C++ benchmarks:  
icpx

Fortran benchmarks:  
ifort
Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX_X64</td>
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<tr>
<td>502.gcc_r</td>
<td>-DSPEC_LP64</td>
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<tr>
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<tr>
<td>557.xz_r</td>
<td>-DSPEC_LP64</td>
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</tbody>
</table>

Base Optimization Flags

C benchmarks:
-`-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math`
-`-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
-`-mbranches-within-32B-boundaries`
-`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
-`-lqkmalloc`

C++ benchmarks:
-`-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto`
-`-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
-`-mbranches-within-32B-boundaries`
-`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
-`-lqkmalloc`

Fortran benchmarks:
-`-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div`
-`-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`
-`-auto -mbranches-within-32B-boundaries`
-`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
-`-lqkmalloc`

Peak Compiler Invocation

C benchmarks (except as noted below):
`icx`

500.perlbench_r: icc

(Continued on next page)
Peak Compiler Invocation (Continued)

557.xz_r: icc

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Peak Portability Flags

C benchmarks:
500.perlbench_r -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -fto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: basepeak = yes

(Continued on next page)
Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DIT400TR-48RL
(2.10 GHz, Intel Xeon Silver 4216)

SPEC CPU®2017 Integer Rate Result
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Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

SPECrate®2017_int_base = 188
SPECrate®2017_int_peak = 194

Peak Optimization Flags (Continued)

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
520.omnetpp_r: basepeak = yes
523.xalancbmk_r: basepeak = yes
531.deepsjeng_r: basepeak = yes
541.leela_r: basepeak = yes

Fortran benchmarks:
548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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