## SPEC CPU 2017 Floating Point Rate Result

### CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

---

## Hardware

**CPU Name:** Intel Xeon Gold 6336Y  
**Max MHz:** 3600  
**Nominal:** 2400

**Enabled:**
- 48 cores, 2 chips, 2 threads/core
**Orderable:**
- 1,2 Chips

**Cache Levels:**
- L1: 32 KB I + 48 KB D on chip per core
- L2: 1.25 MB I+D on chip per core
- L3: 36 MB I+D on chip per core
**Other:** None

**Memory:** 1 TB (32 x 32 GB 1Rx4 PC4-3200AA-R)

**Storage:** 1 x 250 GB SATA SSD  
**Other:** None

---

## Software

**OS:** CentOS Linux release 8.4.2105  
**Kernel:** 4.18.0-305.3.1.el8.x86_64

**Compiler:**
- C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
- Fortran: Version 2021.1 of Intel Fortran Compiler
- C/C++: Version 2021.1 of Intel C/C++ Compiler

**Parallel:** No  
**Firmware:** Version SE5C620.86B.01.0003.2104260124 released Apr-2021  
**File System:** xfs  
**System State:** Run level 3 (multi-user)

**Base Pointers:** 64-bit  
**Peak Pointers:** 64-bit  
**Other:** jemalloc memory allocator V5.0.1

---

## Results

### SPECrate®2017_fp_base = 319  
### SPECrate®2017_fp_peak = 322

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
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(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero ID1100C2R-28
(2.40 GHz, Intel Xeon Gold 6336Y)

SPECrate®2017_fp_base = 319
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Results Table

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<td>131</td>
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<td>131</td>
<td>1161</td>
<td>131</td>
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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
SPEC CPU®2017 Floating Point Rate Result

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(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero ID1100C2R-28
(2.40 GHz, Intel Xeon Gold 6336Y)

SPECrate®2017_fp_base = 319
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<tr>
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<td>Software Availability: Jun-2021</td>
</tr>
</tbody>
</table>

General Notes

- Binaries compiled locally by Netweb
- Transparent Huge Pages enabled by default
- Prior to runcpu invocation
- Filesystem page cache synced and cleared with:
  ```
  sync; echo 3 > /proc/sys/vm/drop_caches
  numactl --interleave=all runcpu <etc>
  ```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
- Power Technology set to Custom
- Power Performance Tuning set to BIOS Controls EPB
- ENERGY_PERF_BIAS_CFG mode set to Performance
- LLC Dead Line Alloc set to Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on localhost.localdomain Sat Aug 21 22:03:47 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name: Intel(R) Xeon(R) Gold 6336Y CPU @ 2.40GHz
  2 *physical id"s (chips)
  96 *processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores: 24
  siblings: 48
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lscpu from util-linux 2.32.1:

(Continued on next page)
Tyrone Systems
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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

SPECrater®2017_fp_base = 319
SPECrater®2017_fp_peak = 322

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Platform Notes (Continued)

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
BIOS Vendor ID: Intel(R) Corporation
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6336Y CPU @ 2.40GHz
BIOS Model name: Intel(R) Xeon(R) Gold 6336Y CPU @ 2.40GHz
Stepping: 6
CPU MHz: 1510.978
CPU max MHz: 3600.0000
CPU min MHz: 800.0000
BoGoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 36864K
NUMA node0 CPU(s): 0-11, 48-59
NUMA node1 CPU(s): 12-23, 60-71
NUMA node2 CPU(s): 24-35, 72-83
NUMA node3 CPU(s): 36-47, 84-95
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
apermperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_13 invpcid_single ssbd
mba ibrs ibpb stibp ibrs_enhanced fsqsbse tsc_adjust bmi1 hle avx2 smep bmi2 erms
invpcid cmp rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb
intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsavec xgetbv1 xsavees cmpqlc
cmp_occupa llc cmp_mmb_total cmp_mmb_local split_lock_detect wbnoinvd dtherm ida arat
pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vbm1 umip pku ospke
avx512_vbmi2 gfnv vaes vpcmulqdq avx512_vnni avx512_bitalg tme avx512_vpdcntdq
la57 rdpid fsrc md_clear pconfig flush_l1d arch_capabilities

/proc/cpuinfo cache data
cache size: 36864 KB

From numactl --hardware

(Continued on next page)
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Tested by: Tyrone Systems
Hardware Availability: Apr-2021
Software Availability: Jun-2021

Platform Notes (Continued)

WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 48 49 50 51 52 53 54 55 56 57 58 59
node 0 size: 257671 MB
node 0 free: 243893 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 60 61 62 63 64 65 66 67 68 69 70 71
node 1 size: 258042 MB
node 1 free: 248253 MB
node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 72 73 74 75 76 77 78 79 80 81 82 83
node 2 size: 258042 MB
node 2 free: 248052 MB
node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 84 85 86 87 88 89 90 91 92 93 94 95
node 3 size: 258002 MB
node 3 free: 248080 MB
node distances:
node   0   1   2   3
0:  10  11  20  20
1:  11  10  20  20
2:  20  20  10  11
3:  20  20  11  10

From /proc/meminfo
MemTotal:       1056521556 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sbin/tuned-adm active
Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
centos-release: CentOS Linux release 8.4.2105
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.4
os-release:
  NAME="CentOS Linux"
  VERSION="8"
  ID="centos"
  ID_LIKE="rhel fedora"
  VERSION_ID="8"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="CentOS Linux 8"
  ANSI_COLOR="0;31"
redhat-release: CentOS Linux release 8.4.2105
system-release: CentOS Linux release 8.4.2105
system-release-cpe: cpe:/o:centos:centos:8

(Continued on next page)
Platform Notes (Continued)

uname -a:
Linux localhost.localdomain 4.18.0-305.3.1.el8.x86_64 #1 SMP Tue Jun 1 16:14:33 UTC 2021 x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Aug 21 14:17

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/cl-home xfs 163G 108G 55G 67% /home

From /sys/devices/virtual/dmi/id
Vendor: Intel Corporation
Product: WHITLEY
Product Family: Family
Serial: UNKNOWN

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x Micron 18ASF4G72PZ-3G2E1 32 GB 1 rank 3200

BIOS:
  BIOS Vendor: Intel Corporation
  BIOS Version: SE5C620.86B.01.01.0003.2104260124
  BIOS Date: 04/26/2021

(End of data from sysinfo program)
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Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
                  | 544.nab_r(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
==============================================================================
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Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C++, C          | 511.povray_r(peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

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C++, C          | 511.povray_r(base) 526.blender_r(base, peak)
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Compiler Version Notes (Continued)

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________________________________________________________________________

C++, C  | 511.povray_r(base) 526.blender_r(base, peak)

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________________________________________________________________________

C++, C, Fortran | 507.cactuBSSN_r(base, peak)

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Fortran  | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
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________________________________________________________________________

Fortran, C | 521.wrf_r(peak)

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Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
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## Compiler Version Notes (Continued)

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## Base Compiler Invocation

C benchmarks:
- `icx`

C++ benchmarks:
- `icpx`

Fortran benchmarks:
- `ifort`

(Continued on next page)
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</table>

Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort icx
Benchmarks using both C and C++:
icpx icx
Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactusBSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto

(Continued on next page)
Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-fflto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/je5.0.1-64/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-fflto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-fflto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/je5.0.1-64/lib

Peak Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
521.wrf_r:ifort icc
527.cam4_r:ifort icx

Benchmarks using both C and C++:

(Continued on next page)
Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero IDI100C2R-28
(2.40 GHz, Intel Xeon Gold 6336Y)

SPECrater®2017_fp_base = 319
SPECrater®2017_fp_peak = 322

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Jun-2021

Peak Compiler Invocation (Continued)

511.povray_r: icpc icc
526.blender_r: icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags
C benchmarks:
519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-Ofast -qopt-mem-layout-trans=4
-flto-accuracy-bits=14:sqrt
-mbranch-within-32B-boundaries -ljemalloc
-L/usr/local/je5.0.1-64/lib

C++ benchmarks:
508.namd_r: basepeak = yes
510.parest_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/je5.0.1-64/lib

Fortran benchmarks:
503.bwaves_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/je5.0.1-64/lib

(Continued on next page)
Peak Optimization Flags (Continued)

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/je5.0.1-64/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.