Hewlett Packard Enterprise
(Tests Sponsor: HPE)
ProLiant DL380 Gen10 Plus
(2.10 GHz, Intel Xeon Silver 4310)

| SPECrate®2017_int_base = 168 |
| SPECrate®2017_int_peak = 174 |

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base (168)</th>
<th>SPECrate®2017_int_peak (174)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>48</td>
<td>129</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>48</td>
<td>147</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>48</td>
<td>163</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>48</td>
<td>123</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>48</td>
<td>212</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>48</td>
<td>294</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>48</td>
<td>122</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>48</td>
<td>118</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>48</td>
<td>328</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>48</td>
<td>350</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Silver 4310  
- **Max MHz:** 3300  
- **Nominal:** 2100  
- **Enabled:** 24 cores, 2 chips, 2 threads/core  
- **Orderable:** 1, 2 chip(s)  
- **Cache L1:** 32 KB I + 48 KB D on chip per core  
- **L2:** 1.25 MB I+D on chip per core  
- **L3:** 18 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)  
- **Storage:** 1 x 400 GB SAS SSD, RAID 0  
- **Other:** None

**Software**

- **OS:** Red Hat Enterprise Linux 8.3 (Ootpa)  
- **Kernel:** 4.18.0-240.el8.x86_64  
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++  
- **Compiler Build:** 20201113 for Linux;  
- **Fortran:** Version 2021.1 of Intel Fortran Compiler  
- **Parallel:** No  
- **Firmware:** HPE BIOS Version U46 v1.50 05/27/2021 released May-2021  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Base</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>48</td>
<td>693</td>
<td>110</td>
<td>694</td>
<td>110</td>
<td>693</td>
<td>110</td>
<td>694</td>
<td>110</td>
<td>693</td>
<td>110</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>48</td>
<td>461</td>
<td>147</td>
<td>463</td>
<td>147</td>
<td>467</td>
<td>145</td>
<td>467</td>
<td>145</td>
<td>467</td>
<td>145</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>48</td>
<td>264</td>
<td>294</td>
<td>263</td>
<td>295</td>
<td>264</td>
<td>294</td>
<td>264</td>
<td>294</td>
<td>264</td>
<td>294</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>48</td>
<td>512</td>
<td>123</td>
<td>513</td>
<td>123</td>
<td>511</td>
<td>123</td>
<td>511</td>
<td>123</td>
<td>511</td>
<td>123</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>48</td>
<td>240</td>
<td>211</td>
<td>239</td>
<td>212</td>
<td>239</td>
<td>212</td>
<td>239</td>
<td>212</td>
<td>239</td>
<td>212</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>48</td>
<td>252</td>
<td>333</td>
<td>252</td>
<td>333</td>
<td>252</td>
<td>333</td>
<td>252</td>
<td>333</td>
<td>252</td>
<td>333</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>48</td>
<td>452</td>
<td>122</td>
<td>452</td>
<td>122</td>
<td>452</td>
<td>122</td>
<td>452</td>
<td>122</td>
<td>452</td>
<td>122</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>48</td>
<td>672</td>
<td>118</td>
<td>671</td>
<td>119</td>
<td>674</td>
<td>118</td>
<td>671</td>
<td>119</td>
<td>674</td>
<td>118</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>48</td>
<td>383</td>
<td>328</td>
<td>384</td>
<td>328</td>
<td>384</td>
<td>328</td>
<td>384</td>
<td>328</td>
<td>384</td>
<td>328</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>48</td>
<td>554</td>
<td>93.7</td>
<td>554</td>
<td>93.6</td>
<td>554</td>
<td>93.6</td>
<td>554</td>
<td>93.6</td>
<td>554</td>
<td>93.6</td>
</tr>
</tbody>
</table>

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
```
sync; echo 3 > /proc/sys/vm/drop_caches
```

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
```bash
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/jre5.0.1-32"
MALLOCONF = "retain:true"
```

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Red Hat Enterprise Linux 8.1
runcpu command invoked through numactl i.e.:

(Continued on next page)
**General Notes (Continued)**

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


**Platform Notes**

The system ROM used for this result contains Intel microcode version 0xd0002a0 for the Intel Xeon Silver 4310 processor.

BIOS Configuration:
- Workload Profile set to General Throughput Compute
- Memory Patrol Scrubbing set to Disabled
- Advanced Memory Protection set to Advanced ECC
- XPT Remote Prefetcher set to Enabled
- Last Level Cache (LLC) Dead Line Allocation set to Disabled
- Enhanced Processor Performance set to Enabled
- Enhanced Processor Performance Profile set to Aggressive
- Thermal Configuration set to Maximum Cooling
- Intel UPI Link Frequency set to Minimum
- Intel UPI Link Enablement set to Single Link
- D2K set to Disabled
- Workload Profile set to Custom
  - DCU Stream Prefetcher set to Disabled
  - Energy Efficient Turbo set to Enabled
  - Adjacent Sector Prefetch set to Disabled
  - Intel UPI Link Power Management set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on localhost.localdomain Tue Aug 24 05:52:41 2021

SUT (System Under Test) info as seen by some common utilities. For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) Silver 4310 CPU @ 2.10GHz
- 2 "physical id"s (chips)
- 48 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following

(Continued on next page)
<table>
<thead>
<tr>
<th>SPEC CPU®2017 Integer Rate Result</th>
<th>Test Date:</th>
<th>Aug-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hewlett Packard Enterprise</td>
<td>Hardware Availability:</td>
<td>Jun-2021</td>
</tr>
<tr>
<td>(Test Sponsor: HPE)</td>
<td>Software Availability:</td>
<td>Dec-2020</td>
</tr>
<tr>
<td>ProLiant DL380 Gen10 Plus</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(2.10 GHz, Intel Xeon Silver 4310)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CPU2017 License:** 3

**Test Sponsor:** HPE

**Tested by:** HPE

**SPECrate®2017_int_base = 168**

**SPECrate®2017_int_peak = 174**

---

**Platform Notes (Continued)**

excerpt from /proc/cpuinfo might not be reliable. Use with caution.

cpu cores : 12  
siblings : 24  
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11  
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11

From lscpu from util-linux 2.32.1:

Architecture: x86_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  
CPU(s): 48  
On-line CPU(s) list: 0-47  
Thread(s) per core: 2  
Core(s) per socket: 12  
Socket(s): 2  
NUMA node(s): 4  
Vendor ID: GenuineIntel  
CPU family: 6  
Model: 106  
Model name: Intel(R) Xeon(R) Silver 4310 CPU @ 2.10GHz  
Stepping: 6  
CPU MHz: 3083.290  
BogoMIPS: 4200.00  
Virtualization: VT-x  
L1d cache: 48K  
L1l cache: 32K  
L2 cache: 1280K  
L3 cache: 18432K  
NUMA node0 CPU(s): 0-5,24-29  
NUMA node1 CPU(s): 6-11,30-35  
NUMA node2 CPU(s): 12-17,36-41  
NUMA node3 CPU(s): 18-23,42-47  
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsc 
    lm constant_tsc arch_perfmon pebs bts rep_good nopl nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 
    xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd 
    mba ibrs ib MCP ibrs Enhanced tpr_shadow vmi flexpriority ept pvid ept_ad 
    fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets invp ci cqm rdt_a avx512f avx512dq 
    rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsavec xgetbv1 xsave xor xsavec qsm llc qsm_occup llc qsm_mbb total 
    qsm_mbb_local split_lock_detect wbnoivd dtherm ida ar at pin pts avx512v bmi umip pku 
    ospeke avx512_vbmi2 gfn i vaes vcpu1 lqdg avx512 vnni avx512 bitalg tme 
    avx512 vp opcnt dq ia57 rdpid md clear pconfig flush lld arch_capabilities

/proc/cpuinfo cache data

(Continued on next page)
Hewlett Packard Enterprise  
(Test Sponsor: HPE)  
ProLiant DL380 Gen10 Plus  
(2.10 GHz, Intel Xeon Silver 4310)  

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE  
**Test Date:** Aug-2021  
**Hardware Availability:** Jun-2021  
**Software Availability:** Dec-2020  

---  

**SPECrate®2017_int_base = 168**  
**SPECrate®2017_int_peak = 174**  

---  

**Platform Notes (Continued)**

```text
from numactl --hardware  
warning: a numactl 'node' might or might not correspond to a physical chip.  
available: 4 nodes (0-3)  
node 0 cpus: 0 1 2 3 4 5 24 25 26 27 28 29  
node 0 size: 510381 MB  
node 0 free: 515455 MB  
node 1 cpus: 6 7 8 9 10 11 30 31 32 33 34 35  
node 1 size: 510760 MB  
node 1 free: 515821 MB  
node 2 cpus: 12 13 14 15 16 17 36 37 38 39 40 41  
node 2 size: 510644 MB  
node 2 free: 515801 MB  
node 3 cpus: 18 19 20 21 22 23 42 43 44 45 46 47  
node 3 size: 510948 MB  
node 3 free: 515564 MB  
node distances:  
node 0 1 2 3  
0: 10 20 30 30  
1: 20 10 30 30  
2: 30 30 10 20  
3: 30 30 20 10  
```

---  

From `/proc/meminfo`  
MemTotal: 2113491664 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB  
/sbin/tuned-adm active  
Current active profile: throughput-performance  

---  

From `/etc/*release* /etc/*version*`  
```text
os-release:  
NAME="Red Hat Enterprise Linux"  
VERSION="8.3 (Ootpa)"  
ID="rhel"  
ID_LIKE="fedora"  
VERSION_ID="8.3"  
PLATFORM_ID="platform:el8"  
PRETTY_NAME="Red Hat Enterprise Linux 8.3 (Ootpa)"  
ANSI_COLOR="0;31"  
redhat-release: Red Hat Enterprise Linux release 8.3 (Ootpa)  
system-release: Red Hat Enterprise Linux release 8.3 (Ootpa)  
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.3:ga  
uname -a:  
```

---  

(Continued on next page)
Platform Notes (Continued)

Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Wed Sep 23 05:13:10 EDT 2020
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swaps barrier and __user pointer sanitization
CVE-2017-5753 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2017-5715 (Spectre variant 2): Not affected
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Aug 24 05:51

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs 297G 103G 195G 35% /home

From /sys/devices/virtual/dmi/id
Vendor: HPE
Product: ProLiant DL380 Gen10 Plus
Product Family: ProLiant
Serial: CN70110BZV

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x Micron 36ASF8G72PZ-3G2B2 64 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: HPE
BIOS Version: U46
BIOS Date: 05/27/2021
BIOS Revision: 1.50
Firmware Revision: 2.50

(End of data from sysinfo program)
Hewlett Packard Enterprise  
(Test Sponsor: HPE)  
ProLiant DL380 Gen10 Plus  
(2.10 GHz, Intel Xeon Silver 4310)  

SPECCPU®2017 Integer Rate Result  
Copyright 2017-2021 Standard Performance Evaluation Corporation

CPU2017 License: 3  
Test Sponsor: HPE  
Tested by: HPE

SPECrater®2017_int_base = 168  
SPECrater®2017_int_peak = 174

Test Date: Aug-2021  
Hardware Availability: Jun-2021  
Software Availability: Dec-2020

Compiler Version Notes

==============================================================================
C       | 500.perlbench_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================
C       | 502.gcc_r(peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version  
2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)  
| 525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================
C       | 500.perlbench_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================
C       | 502.gcc_r(peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version  
2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)  
| 525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10 Plus
(2.10 GHz, Intel Xeon Silver 4310)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 168
SPECrate®2017_int_peak = 174

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--

C           | 500.perlbench_r(peak)
--
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--

C           | 502.gcc_r(peak)
--
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--

C           | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
--
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--

C++         | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
--
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--

Fortran      | 548.exchange2_r(base, peak)
--
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Hewlett Packard Enterprise (Test Sponsor: HPE)
ProLiant DL380 Gen10 Plus (2.10 GHz, Intel Xeon Silver 4310)

SPECrate®2017_int_base = 168
SPECrate®2017_int_peak = 174

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Hewlett Packard Enterprise
ProLiant DL380 Gen10 Plus
(2.10 GHz, Intel Xeon Silver 4310)

SPECrate®2017_int_base = 168
SPECrate®2017_int_peak = 174

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Aug-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

Base Optimization Flags (Continued)

Fortran benchmarks (continued):
- L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
- lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icx
500.perlbench_r: icc

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

(Continued on next page)
# SPEC CPU®2017 Integer Rate Result

## Hewlett Packard Enterprise

### ProLiant DL380 Gen10 Plus

(2.10 GHz, Intel Xeon Silver 4310)

| SPECrate®2017_int_base | 168          |
| SPECrate®2017_int_peak | 174          |

| CPU2017 License: | 3          |
| Test Sponsor:   | HPE        |
| Tested by:      | HPE        |
| Test Date:      | Aug-2021   |
| Hardware Availability: | Jun-2021 |
| Software Availability: | Dec-2020 |

### Peak Optimization Flags (Continued)

```bash
502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass1)
-fprofile-use=default.profdata(pass2) -xcORE-AVX512 -flto
-Ofast(pass1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xcORE-AVX512 -flto
-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: basepeak = yes

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes
```

The flags files that were used to format this result can be browsed at

- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revE.html](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revE.html)

You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revE.xml](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revE.xml)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10 Plus
(2.10 GHz, Intel Xeon Silver 4310)

SPECrater®2017_int_base = 168
SPECrater®2017_int_peak = 174

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Aug-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

SPEC CPU and SPECrater are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU*2017 v1.1.8 on 2021-08-23 20:22:40-0400.
Report generated on 2021-09-14 19:17:56 by CPU2017 PDF formatter v6442.
Originally published on 2021-09-14.