## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

**Cisco UCS B200 M6 (Intel Xeon Gold 5318N, 2.10GHz)**

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>311</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>322</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2021  
**Hardware Availability:** Apr-2021  
**Software Availability:** Dec-2020

### Hardware

- **CPU Name:** Intel Xeon Gold 5318N  
- **Max MHz:** 3400  
- **Nominal:** 2100  
- **Enabled:** 48 cores, 2 chips, 2 threads/core  
- **Orderable:** 1.2 Chips  
- **Cache L1:** 32 KB I + 48 KB D on chip per core  
- **L2:** 1.25 MB I+D on chip per core  
- **L3:** 36 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2666)  
- **Storage:** 1 x 960 GB M.2 SSD SATA  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default  
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++, Classic Build 20201112 for Linux;  
  Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;  
  C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux  
- **Parallel:** No  
- **Firmware:** Version 4.2.1d released Jul-2021  
- **File System:** btrfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage

---

### Benchmarks

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_r</td>
<td>96</td>
<td>213</td>
<td>249</td>
</tr>
<tr>
<td>gcc_r</td>
<td>96</td>
<td>252</td>
<td>512</td>
</tr>
<tr>
<td>mcf_r</td>
<td>96</td>
<td>294</td>
<td></td>
</tr>
<tr>
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<td>96</td>
<td>193</td>
<td></td>
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<td></td>
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<td></td>
<td>636</td>
</tr>
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<td>96</td>
<td></td>
<td>665</td>
</tr>
<tr>
<td>leela_r</td>
<td>96</td>
<td></td>
<td></td>
</tr>
<tr>
<td>exchange2_r</td>
<td>96</td>
<td></td>
<td>655</td>
</tr>
<tr>
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<td></td>
<td></td>
</tr>
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**SPECrate®2017_int_peak:** 322
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5318N, 2.10GHz)

SPECrate®2017_int_base = 311
SPECrate®2017_int_peak = 322

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Base</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>96</td>
<td>718</td>
<td>213</td>
<td>718</td>
<td>213</td>
<td>718</td>
<td>213</td>
<td>96</td>
<td>613</td>
<td>249</td>
<td>613</td>
<td>249</td>
<td>614</td>
<td>249</td>
<td>614</td>
<td>249</td>
<td></td>
<td></td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>96</td>
<td>539</td>
<td>252</td>
<td>541</td>
<td>251</td>
<td>540</td>
<td>252</td>
<td>96</td>
<td>462</td>
<td>294</td>
<td>463</td>
<td>294</td>
<td>462</td>
<td>294</td>
<td>462</td>
<td>294</td>
<td></td>
<td></td>
</tr>
<tr>
<td>505.mcfc_r</td>
<td>96</td>
<td>303</td>
<td>512</td>
<td>304</td>
<td>510</td>
<td>303</td>
<td>512</td>
<td>96</td>
<td>303</td>
<td>512</td>
<td>304</td>
<td>510</td>
<td>303</td>
<td>512</td>
<td>303</td>
<td>512</td>
<td></td>
<td></td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>96</td>
<td>652</td>
<td>193</td>
<td>651</td>
<td>193</td>
<td>651</td>
<td>193</td>
<td>96</td>
<td>652</td>
<td>193</td>
<td>651</td>
<td>193</td>
<td>651</td>
<td>193</td>
<td>651</td>
<td>193</td>
<td></td>
<td></td>
</tr>
<tr>
<td>523.xalanbmk_r</td>
<td>96</td>
<td>261</td>
<td>388</td>
<td>260</td>
<td>390</td>
<td>261</td>
<td>389</td>
<td>96</td>
<td>261</td>
<td>388</td>
<td>260</td>
<td>390</td>
<td>261</td>
<td>389</td>
<td>261</td>
<td>389</td>
<td></td>
<td></td>
</tr>
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<td>96</td>
<td>264</td>
<td>636</td>
<td>264</td>
<td>636</td>
<td>264</td>
<td>636</td>
<td>96</td>
<td>253</td>
<td>666</td>
<td>253</td>
<td>664</td>
<td>253</td>
<td>665</td>
<td>253</td>
<td>665</td>
<td></td>
<td></td>
</tr>
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<td>96</td>
<td>385</td>
<td>653</td>
<td>384</td>
<td>655</td>
<td>384</td>
<td>655</td>
<td>96</td>
<td>385</td>
<td>653</td>
<td>384</td>
<td>655</td>
<td>384</td>
<td>655</td>
<td>384</td>
<td>655</td>
<td></td>
<td></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>96</td>
<td>588</td>
<td>176</td>
<td>586</td>
<td>177</td>
<td>586</td>
<td>177</td>
<td>96</td>
<td>590</td>
<td>176</td>
<td>589</td>
<td>176</td>
<td>589</td>
<td>176</td>
<td>589</td>
<td>176</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOCONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5318N, 2.10GHz)  

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 311</th>
<th>Test Date: Aug-2021</th>
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<tr>
<td>SPECrate®2017_int_peak = 322</td>
<td>Hardware Availability: Apr-2021</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  

General Notes (Continued)

runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acfc64d  
running on localhost Fri Aug 27 04:14:18 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5318N CPU @ 2.10GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

(Continued on next page)
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Test Date: Aug-2021
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Hardware Availability: Apr-2021
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Platform Notes (Continued)

From /proc/cpuinfo:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 5318N CPU @ 2.10GHz
Stepping: 6
CPU MHz: 1606.211
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 36864K
NUMA node0 CPU(s): 0-11,48-59
NUMA node1 CPU(s): 12-23,60-71
NUMA node2 CPU(s): 24-35,72-83
NUMA node3 CPU(s): 36-47,84-95
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs tamil tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets emm invpcid_single ssbd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets emm invpcid_single ssbd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets emm invpcid_single ssbd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase
cache size: 36864 KB

(Continued on next page)
Platform Notes (Continued)

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 48 49 50 51 52 53 54 55 56 57 58 59
node 0 size: 257371 MB
node 0 free: 257027 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 60 61 62 63 64 65 66 67 68 69 70 71
node 1 size: 258042 MB
node 1 free: 257588 MB
node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 72 73 74 75 76 77 78 79 80 81 82 83
node 2 size: 258042 MB
node 2 free: 257721 MB
node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 84 85 86 87 88 89 90 91 92 93 94 95
node 3 size: 257763 MB
node 3 free: 257459 MB
node distances:

node 0 1 2 3
0: 10 11 20 20
1: 11 10 20 20
2: 20 20 10 11
3: 20 20 11 10

From /proc/meminfo
MemTotal: 1055969396 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
oS-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5318N, 2.10GHz)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 311
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
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Platform Notes (Continued)

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store
CVE-2018-3639 (Speculative Store Bypass): Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs
CVE-2017-5715 (Spectre variant 2): barriers and __user pointer
CVE-2020-0543 (Special Register Buffer Data Sampling): Mitigation: Enhanced IBRS, IBPB:
CVE-2019-11135 (TSX Asynchronous Abort): conditional, RSB filling

run-level 3 Aug 27 04:12
SPEC is set to: /home/cpu2017

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH24097570

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: B200M6.4.2.1d.0.0730210924
BIOS Date: 07/30/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 500.perlbench_r(peak) 557.xz_r(peak)
==============================================================================

(Continued on next page)
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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
| C       | 502.gcc_r(peak) |
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
| C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base) |
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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| C       | 500.perlbench_r(peak) 557.xz_r(peak) |
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Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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| C       | 502.gcc_r(peak) |
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**SPEC CPU®2017 Integer Rate Result**  

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**Compiler Version Notes (Continued)**

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**C**  
| 500.perlbench_r(peak) 557.xz_r(peak)  

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Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000  
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**C**  
| 502.gcc_r(peak)  

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---

**C**  
| 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)  
| 525.x264_r(base, peak) 557.xz_r(base)  

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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113  
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**C++**  
| 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)  
| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)  

---

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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**Fortran**  
| 548.exchange2_r(base, peak)  

---

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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**SPECrate®2017_int_base = 311**  
**SPECrate®2017_int_peak = 322**
## Base Compiler Invocation

| C benchmarks: | icx |
| C++ benchmarks: | icpx |
| Fortran benchmarks: | ifort |

## Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>gcc_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>mcf_r</td>
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</tr>
<tr>
<td>xz_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>(Continued on next page)</td>
<td></td>
</tr>
</tbody>
</table>

## Base Optimization Flags

<table>
<thead>
<tr>
<th>C benchmarks:</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>-w</td>
<td>-m64</td>
</tr>
<tr>
<td>-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4</td>
<td></td>
</tr>
<tr>
<td>-mbranches-within-32B-boundaries</td>
<td></td>
</tr>
<tr>
<td>-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin</td>
<td></td>
</tr>
<tr>
<td>-lgqkmalloc</td>
<td></td>
</tr>
</tbody>
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<table>
<thead>
<tr>
<th>C++ benchmarks:</th>
<th>Flags</th>
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<tbody>
<tr>
<td>-w</td>
<td>-m64</td>
</tr>
<tr>
<td>-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4</td>
<td></td>
</tr>
<tr>
<td>-mbranches-within-32B-boundaries</td>
<td></td>
</tr>
<tr>
<td>-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin</td>
<td></td>
</tr>
<tr>
<td>-lgqkmalloc</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fortran benchmarks:</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div</td>
<td></td>
</tr>
<tr>
<td>-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte</td>
<td></td>
</tr>
<tr>
<td>-auto -mbranches-within-32B-boundaries</td>
<td></td>
</tr>
</tbody>
</table>

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Cisco Systems  
Cisco UCS B200 M6 (Intel Xeon Gold 5318N, 2.10GHz)  

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 311</th>
<th>SPECrate®2017_int_peak = 322</th>
</tr>
</thead>
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<td>Software Availability: Dec-2020</td>
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</table>

**Base Optimization Flags (Continued)**

Fortran benchmarks (continued):
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

**Peak Compiler Invocation**

C benchmarks (except as noted below):
- `icx`
- `500.perlbench_r:icc`
- `557.xz_r:icc`

C++ benchmarks:
- `icpx`

Fortran benchmarks:
- `ifort`

**Peak Portability Flags**

500.perlbench_r `-DSPEC_LP64 -DSPEC_LINUX_X64`
502.gcc_r `-D_FILE_OFFSET_BITS=64`
505.mcf_r `-DSPEC_LP64`
520.omnetpp_r `-DSPEC_LP64`
523.xalancbmk_r `-DSPEC_LP64 -DSPEC_LINUX`
525.x264_r `-DSPEC_LP64`
531.deepsjeng_r `-DSPEC_LP64`
541.leela_r `-DSPEC_LP64`
548.exchange2_r `-DSPEC_LP64`
557.xz_r `-DSPEC_LP64`

**Peak Optimization Flags**

C benchmarks:
- `500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)`
- `-xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4 -fno-strict-overflow`
- `-mbranches-within-32B-boundaries`

(Continued on next page)
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SPEC CPU®2017 Integer Rate Result
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Peak Optimization Flags (Continued)

500.perlbench_r (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w
-std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
520.omnetpp_r: basepeak = yes
523.xalancbmk_r: basepeak = yes
531.deepsjeng_r: basepeak = yes
541.leela_r: basepeak = yes

Fortran benchmarks:
548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**  
Cisco UCS B20! M6 (Intel Xeon Gold 5318N, 2.10GHz)  

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Tested with SPEC CPU®2017 v1.1.8 on 2021-08-27 07:14:18-0400.  
Originally published on 2021-09-14.