Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5318Y, 2.10GHz)

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<th>315</th>
<th>SPECrate®2017_fp_peak = Not Run</th>
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</thead>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

### Hardware

| Copies | 0 | 40.0 | 80.0 | 120 | 160 | 200 | 240 | 280 | 320 | 360 | 400 | 440 | 480 | 520 | 560 | 600 | 640 | 680 | 720 | 760 | 800 | 810 |
|--------|---|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 503.bwaves_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 507.cactuBSSN_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 508.namd_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 510.parest_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 511.povray_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 519.lbm_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 521.wrf_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 526.blender_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 527.cam4_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 538.imagick_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 544.nab_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 549.fotonik3d_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 554.roms_r | 96 |       |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

### Software

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Gold 5318Y</td>
<td>OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default</td>
</tr>
<tr>
<td>Max MHz: 3400</td>
<td>Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux</td>
</tr>
<tr>
<td>Nominal: 2100</td>
<td>Parallel: No</td>
</tr>
<tr>
<td>Enabled: 48 cores, 2 chips, 2 threads/core</td>
<td>Firmware: Version 4.2.1d released Jul-2021</td>
</tr>
<tr>
<td>Orderable: 1,2 Chips</td>
<td>File System: btrfs</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 48 KB D on chip per core</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>L2: 1.25 MB I+D on chip per core</td>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>L3: 36 MB I+D on chip per chip</td>
<td>Peak Pointers: Not Applicable</td>
</tr>
<tr>
<td>Other: None</td>
<td>Other: jemalloc memory allocator V5.0.1</td>
</tr>
<tr>
<td>Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2933)</td>
<td>Power Management: BIOS and OS set to prefer performance at the cost of additional power usage</td>
</tr>
<tr>
<td>Storage: 1 x 960 GB M.2 SSD SATA</td>
<td></td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5318Y, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrater®2017_fp_base = 315
SPECrater®2017_fp_peak = Not Run

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

---

## Results Table

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<td>137</td>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCONF = "retain:true"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using opensUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5318Y, 2.10GHz)

SPECrat®2017_fp_base = 315
SPECrat®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

General Notes (Continued)

sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
    numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDC Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on localhost Wed Aug 25 18:08:17 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 5318Y CPU @ 2.10GHz
    2 "physical id"s (chips)
    96 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 24
    siblings : 48
    physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
    physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lsmpu from util-linux 2.33.1:
    Architecture: x86_64

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5318Y, 2.10GHz)

Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_fp_base = 315
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2021
Tested by: Cisco Systems
Hardware Availability: Apr-2021
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Platform Notes (Continued)

CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 5318Y CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2818.884
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 36864K
NUMA node0 CPU(s): 0-11,48-59
NUMA node1 CPU(s): 12-23,60-71
NUMA node2 CPU(s): 24-35,72-83
NUMA node3 CPU(s): 36-47,84-95
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aerpmpref perf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd
mba ibpb stibp ibrs_enhanced tpr_shadow vmoi flexpriority ept vpid ept_ad
fsigsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni
avx512vw avx512vl xsaveopt xsaves xsavec xgetbv1 xsaveaves cqm_llc cqm_occup_llc cqm_mbm_total
qm_mbm_local wbinvd dtherm ida arat pln pts hwp hwp_act_window hwlp epp
hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfini vaes vpclmulqdq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfug flush_l1d
arch_capabilities

/platforminfo cache data
  cache size : 36864 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5318Y, 2.10GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECRate®2017_fp_base = 315
SPECRate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Platform Notes (Continued)

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 48 49 50 51 52 53 54 55 56 57 58 59
node 0 size: 257405 MB
node 0 free: 256978 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 60 61 62 63 64 65 66 67 68 69 70 71
node 1 size: 258008 MB
node 1 free: 257612 MB
node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 72 73 74 75 76 77 78 79 80 81 82 83
node 2 size: 258042 MB
node 2 free: 257790 MB
node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 84 85 86 87 88 89 90 91 92 93 94 95
node 3 size: 257763 MB
node 3 free: 257485 MB
node distances:
node 0   1   2   3
0:  10  11  20  20
1:  11  10  20  20
2:  20  20  10  11
3:  20  20  11  10

From /proc/meminfo
MemTotal:       1055969400 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
  NAME="SLES"
  VERSION="15-SP2"
  VERSION_ID="15.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5318Y, 2.10GHz)

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Platform Notes (Continued)

Microarchitectural Data Sampling:
- Not affected
- Not affected
- Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- Mitigation: usercopy/swaps barriers and __user pointer sanitation
- Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2017-5753 (Spectre variant 1):
- Not affected

CVE-2017-5715 (Spectre variant 2):
- Not affected

CVE-2020-0543 (Special Register Buffer Data Sampling):
- Not affected

CVE-2019-11135 (TSX Asynchronous Abort):
- Not affected

run-level 3 Aug 25 18:06
SPEC is set to: /home/cpu2017
Filesistem     Type   Size  Used Avail Use% Mounted on
/dev/sda3      btrfs  603G  9.0G  592G   2% /home

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2933

BIOS:
- BIOS Vendor: Cisco Systems, Inc.
- BIOS Version: B200M6.4.2.1d.0.0730210924
- BIOS Date: 07/30/2021
- BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

---
C | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
---

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113

(Continued on next page)
## Cisco Systems

**Cisco UCS B200 M6 (Intel Xeon Gold 5318Y, 2.10GHz)**

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**SPECrate®2017_fp_base = 315**

**SPECrate®2017_fp_peak = Not Run**

---

### Compiler Version Notes (Continued)

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| C++ | 508.namd_r(base) 510.parest_r(base) |
|--------------------------------------|
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |

---

| C++, C | 511.povray_r(base) 526.blender_r(base) |
|----------------------------------------|
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113 |
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<tbody>
<tr>
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## Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Gold 5318Y, 2.10GHz)

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**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

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**Software Availability:** Dec-2020

### Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000

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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113

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---

### Base Compiler Invocation

**C benchmarks:**

icx

**C++ benchmarks:**

icpx

**Fortran benchmarks:**

ifort

**Benchmarks using both Fortran and C:**

ifort icx

**Benchmarks using both C and C++:**

icpx icx

**Benchmarks using Fortran, C, and C++:**

icpx icx ifort

### Base Portability Flags

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.namd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.ibm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5318Y, 2.10GHz)

SPECrates®
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Spec CPU®2017 Floating Point Rate Result
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Base Optimization Flags

C benchmarks:
- w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
- flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- mbranches-within-32B-boundaries -ljemalloc
- L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
- w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
- mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- mbranches-within-32B-boundaries -ljemalloc
- L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
- w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
- nostandard-realloc-lhs -align array32byte -auto
- mbranches-within-32B-boundaries -ljemalloc
- L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
- w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
- flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
- no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles
- mbranches-within-32B-boundaries -nostandard-realloc-lhs
- align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
- w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
- flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- mbranches-within-32B-boundaries -ljemalloc
- L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
- w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
- flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
- no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles
- mbranches-within-32B-boundaries -nostandard-realloc-lhs
- align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at
### SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**  
Cisco UCS B200 M6 (Intel Xeon Gold 5318Y, 2.10GHz)

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You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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