Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

SPECspeed®2017_int_base = 11.3
SPECspeed®2017_int_peak = 11.5

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Jun-2021

Software
OS: SUSE Linux Enterprise Server 15 SP2
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
Parallel: Yes
Firmware: Version 4.2.1d released Jul-2021
File System: brfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage

Hardware
CPU Name: Intel Xeon Silver 4316
Max MHz: 3400
Nominal: 2300
Enabled: 40 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 30 MB I+D on chip per chip
Other: None
Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2666)
Storage: 1 x 240 GB SATA SSD
Other: None

Threads

600.perlbench_s 40
602.gcc_s 40
605.mcf_s 40
620.omnetpp_s 40
623.xalancbmk_s 40
625.x264_s 40
631.deepsjeng_s 40
641.leela_s 40
648.exchange2_s 40
657.xz_s 40

SPECspeed®2017_int_base (11.3)
SPECspeed®2017_int_peak (11.5)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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SPECspeed®2017_int_base = 11.3
SPECspeed®2017_int_peak = 11.5

Test Date: Aug-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

Results Table

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<td>657.xz_s</td>
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<td>283</td>
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<td>281</td>
<td>22.0</td>
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</tbody>
</table>

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCS_CONF = "retain: true"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocatio
Filesistem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

SPEC®2017_int_base = 11.3
SPEC®2017_int_peak = 11.5

General Notes (Continued)

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Disabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparring set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled
Intel Hyper-Threading Technology set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on localhost Tue Aug 24 17:47:57 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 20
siblings: 20
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 40
On-line CPU(s) list: 0-39

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

SPEC CPU®2017 Integer Speed Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECspeed®2017_int_base = 11.3
SPECspeed®2017_int_peak = 11.5

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2021
Tested by: Cisco Systems
Software Availability: Dec-2020
Hardware Availability: Jun-2021

Platform Notes (Continued)

Thread(s) per core: 1
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz
Stepping: 6
CPU MHz: 1591.144
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 30720K
NUMA node0 CPU(s): 0-19
NUMA node1 CPU(s): 20-39

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmprefetch pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd
mrb ibrs stibp ibrs_enhanced tpr_shadow vmi fpu flexpriority ept vpid ept_ad
fsa fgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma pclflushopt clwb intel_pt avx512cd sha_ni
avx512bw avx512vl xsaveopt xsavec xsaveopt xsaves cqm_llc cqm_occu_l1c cqm_mbb_total
#m_mbb_local wbnoiwvd dtherm ida arat pln ptt vts hwp hwp_act_window hwp_epp
hwp_pkg Req avx512vbm umip pku ospke avx512_vbmi2 gfnf vaes vpcmlduqavx512_vnni
avx512_vbitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
arch_capabilities

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
node 0 size: 515650 MB
node 0 free: 514963 MB
node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
node 1 size: 516087 MB
node 1 free: 515604 MB

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

SPEC CPU®2017 Integer Speed Result

SPECspeed®2017_int_base = 11.3
SPECspeed®2017_int_peak = 11.5

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

node distances:
node  0   1
  0:  10   20
  1:  20   10

From /proc/meminfo
MemTotal: 1056499796 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Aug 24 17:42

(Continued on next page)
**Cisco Systems**
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

**SPEC®2017 int_base = 11.3**
**SPEC®2017 int_peak = 11.5**

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Aug-2021  
**Hardware Availability:** Jun-2021  
**Tested by:** Cisco Systems  
**Software Availability:** Dec-2020

---

**Platform Notes (Continued)**

SPEC is set to: /home/cpu2017
Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sdb2      btrfs  222G   57G  165G  26% /home

From /sys/devices/virtual/dmi/id
Vendor:         Cisco Systems Inc
Product:        UCSC-C220-M6S
Serial:         WZP244104TF

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor:     Cisco Systems, Inc.
BIOS Version:    C220M6.4.2.1d.0.0730210924
BIOS Date:       07/30/2021
BIOS Revision:   5.22

(End of data from sysinfo program)

---

**Compiler Version Notes**

```
C       | 600.perlbench_s(peak)
```

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
C       | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
C       | 600.perlbench_s(peak)
```

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

SPECspeed®2017_int_base = 11.3
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CPU2017 License: 9019
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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C       | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
       | 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++     | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
       | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
==============================================================================

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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==============================================================================
Fortran | 648.exchange2_s(base, peak)
==============================================================================

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

| SPECspeed®2017_int_base = 11.3 |
| SPECspeed®2017_int_peak = 11.5 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

### Base Portability Flags

- 600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
- 602.gcc_s: -DSPEC_LP64
- 605.mcf_s: -DSPEC_LP64
- 620.omnetpp_s: -DSPEC_LP64
- 623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
- 625.x264_s: -DSPEC_LP64
- 631.deepsjeng_s: -DSPEC_LP64
- 641.leela_s: -DSPEC_LP64
- 648.exchange2_s: -DSPEC_LP64
- 657.xz_s: -DSPEC_LP64

### Base Optimization Flags

- C benchmarks:
  - -DSPEC_OPENMP -std=c11 -m64 -fopenmp -Wl,-z,muldefs -xCORE-AVX512
  - -O3 -ffast-math -flto -mfpmath=sse -funroll-loops
  - -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
  - -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

- C++ benchmarks:
  - -DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
  - -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
  - -mbranches-within-32B-boundaries
  - -L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/
  - -lqkmalloc

- Fortran benchmarks:
  - -m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
  - -nostandard-realloc-lhs -align array32byte -auto
  - -mbranches-within-32B-boundaries

### Peak Compiler Invocation

- C benchmarks (except as noted below):
  - icx
  - 600.perlbench_s: icc

- C++ benchmarks:
  - icpx

(Continued on next page)
## Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

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### SPECspeed®2017_int_base = 11.3
### SPECspeed®2017_int_peak = 11.5

---

## Peak Compiler Invocation (Continued)

Fortran benchmarks:

- ifort

---

## Peak Portability Flags

Same as Base Portability Flags

---

## Peak Optimization Flags

C benchmarks:

- **600.perlbench_s**:
  - `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)`
  - `-xCORE-AVX512 -ipo -O3 -no-prec-div`
  - `-qopt-mem-layout-trans=4 -fno-strict-overflow`
  - `-mbranches-within-32B-boundaries`
  - `-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

- **602.gcc_s**:
  - `-m64 -std=c11 -Wl,-z,muldefs -fprofile-generate(pass 1)`
  - `-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto`
  - `-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4`
  - `-mbranches-within-32B-boundaries`
  - `-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

- **605.mcf_s**:
  - `basepeak = yes`

- **625.x264_s**:
  - `-DSPEC_OPENMP -fiopenmp -std=c11 -m64 -Wl,-z,muldefs`
  - `-xCORE-AVX512 -flto -O3 -ffast-math`
  - `-qopt-mem-layout-trans=4 -fno-alias`
  - `-mbranches-within-32B-boundaries`
  - `-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

- **657.xz_s**:
  - `basepeak = yes`

C++ benchmarks:

- **620.omnetpp_s**:
  - `basepeak = yes`

- **623.xalancbmk_s**:
  - `basepeak = yes`

- **631.deepsjeng_s**:
  - `basepeak = yes`

---

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

SPECspeed®2017_int_base = 11.3
SPECspeed®2017_int_peak = 11.5

Peak Optimization Flags (Continued)

641.leela_s: basepeak = yes

Fortran benchmarks:
648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-08-24 20:47:57-0400.
Originally published on 2021-09-14.