### Hardware

- **CPU Name:** Intel Xeon Gold 6326  
  - **Max MHz:** 3500  
  - **Nominal:** 2900  
  - **Enabled:** 32 cores, 2 chips, 2 threads/core  
  - **Orderable:** 1.2 Chips  
  - **Cache L1:** 32 KB I + 48 KB D on chip per core  
  - **L2:** 1.25 MB I+D on chip per core  
  - **L3:** 24 MB I+D on chip per chip  
  - **Other:** None  
- **Memory:** 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R)  
- **Storage:** 1 x 240 GB SATA SSD  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 SP2  
  - 5.3.18-22-default  
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;  
  - Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;  
  - C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux  
- **Parallel:** No  
- **Firmware:** Version 4.2.1c released Jul-2021  
- **File System:** btrfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage

### Test Information

- **CPU2017 License:** 9019  
- **Test Sponsor:** Cisco Systems  
- **Test Date:** Aug-2021  
- **Hardware Availability:** Jun-2021  
- **Tested by:** Cisco Systems  
- **Software Availability:** Dec-2020

### Benchmark Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECRate®2017_int_base</th>
<th>SPECRate®2017_int_peak</th>
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<td>500.perlbench_r</td>
<td>64</td>
<td>205</td>
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<td>502.gcc_r</td>
<td>64</td>
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Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6326, 2.90GHz)

SPECrater®2017_int_base = 260
SPECrater®2017_int_peak = 268

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

| Benchmark          | Copies | Seconds | Ratio | Base             | Copies | Seconds | Ratio | Peak             | Copies | Seconds | Ratio | Base             | Copies | Seconds | Ratio | Peak             | Copies | Seconds | Ratio | Base             | Copies | Seconds | Ratio | Peak             | Copies | Seconds | Ratio | Base             | Copies | Seconds | Ratio | Peak             |
|--------------------|--------|---------|-------|-----------------|--------|----------|-------|-----------------|--------|----------|-------|-----------------|--------|----------|-------|-----------------|--------|----------|-------|-----------------|--------|----------|-------|-----------------|--------|----------|-------|-----------------|--------|----------|-------|-----------------|--------|----------|-------|-----------------|
| 500.perlbench_r    | 64     | 580     | 176   | 580 176         | 64     | 496      | 205   | 497 205         | 64     | 496      | 205   | 497 205         | 64     | 496      | 205   | 497 205         | 64     | 496      | 205   | 497 205         |
| 502.gcc_r          | 64     | 421     | 215   | 422 215         | 64     | 366      | 247   | 366 247         | 64     | 366      | 247   | 366 247         | 64     | 366      | 247   | 366 247         | 64     | 366      | 247   | 366 247         |
| 505.mcf_r          | 64     | 234     | 441   | 235 439         | 64     | 234      | 441   | 235 439         | 64     | 234      | 441   | 235 439         | 64     | 234      | 441   | 235 439         | 64     | 234      | 441   | 235 439         |
| 520.omnetpp_r      | 64     | 519     | 162   | 519 162         | 64     | 519      | 162   | 519 162         | 64     | 519      | 162   | 519 162         | 64     | 519      | 162   | 519 162         | 64     | 519      | 162   | 519 162         |
| 532.xalancbmk_r    | 64     | 205     | 330   | 204 331         | 64     | 205      | 330   | 204 331         | 64     | 205      | 330   | 204 331         | 64     | 205      | 330   | 204 331         | 64     | 205      | 330   | 204 331         |
| 525.x264_r         | 64     | 210     | 533   | 211 532         | 64     | 202      | 554   | 201 557         | 64     | 202      | 554   | 201 557         | 64     | 202      | 554   | 201 557         | 64     | 202      | 554   | 201 557         |
| 531.deepsjeng_r    | 64     | 371     | 198   | 371 198         | 64     | 371      | 198   | 371 198         | 64     | 371      | 198   | 371 198         | 64     | 371      | 198   | 371 198         | 64     | 371      | 198   | 371 198         |
| 541.leela_r        | 64     | 548     | 193   | 549 193         | 64     | 548      | 193   | 549 193         | 64     | 548      | 193   | 549 193         | 64     | 548      | 193   | 549 193         | 64     | 548      | 193   | 549 193         |
| 548.exchange2_r    | 64     | 314     | 535   | 314 535         | 64     | 314      | 535   | 314 535         | 64     | 314      | 535   | 314 535         | 64     | 314      | 535   | 314 535         | 64     | 314      | 535   | 314 535         |
| 557.xz_r           | 64     | 483     | 143   | 483 143         | 64     | 492      | 140   | 492 141         | 64     | 492      | 140   | 492 141         | 64     | 492      | 140   | 492 141         | 64     | 492      | 140   | 492 141         |

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
    "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOC_CONF = "retain:true"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using opensUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6326, 2.90GHz)  

General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on localhost Mon Aug 16 23:54:21 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6326 CPU @ 2.90GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6326, 2.90GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2021
Tested by: Cisco Systems
Hardware Availability: Jun-2021
Software Availability: Dec-2020

Platform Notes (Continued)

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6326 CPU @ 2.90GHz
Stepping: 6
CPU MHz: 800.000
CPU max MHz: 3500.0000
CPU min MHz: 800.0000
BogoMIPS: 5800.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 24576K
NUMA node0 CPU(s): 0-7,32-39
NUMA node1 CPU(s): 8-15,40-47
NUMA node2 CPU(s): 16-23,48-55
NUMA node3 CPU(s): 24-31,56-63
Flags: fpu vme de pse tsc msr pae mce cmov pat aprmnum aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd mba ibrs ibp bts ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase ts_cref tsc_adjust bmi1 hle avx2 smep bmi2 2em ems invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma cmov clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsavec xgetbv1 xsavec cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local wbnoivd dtherm ida rat pln pts hwp_act_window hwp_epp hwp_pkg_rej avx512vbm umip pkc ospke avx512_vbmi2 gfn vaes vpmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md_clear pconfig flush_l1d arch_capabilities

/proc/cpuinfo cache data
cache size : 24576 KB

(Continued on next page)
CISCO SYSTEMS
Cisco UCS C220 M6 (Intel Xeon Gold 6326, 2.90GHz)

| SPECrate®2017_int_base = 260 |
| SPECrate®2017_int_peak = 268 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2021
Tested by: Cisco Systems
Hardware Availability: Jun-2021
Software Availability: Dec-2020

Platform Notes (Continued)

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 32 33 34 35 36 37 38 39
node 0 size: 257637 MB
node 0 free: 257294 MB
node 1 cpus: 8 9 10 11 12 13 14 15 40 41 42 43 44 45 46 47
node 1 size: 258043 MB
node 1 free: 257581 MB
node 2 cpus: 16 17 18 19 20 21 22 23 48 49 50 51 52 53 54 55
node 2 size: 258010 MB
node 2 free: 257775 MB
node 3 cpus: 24 25 26 27 28 29 30 31 56 57 58 59 60 61 62 63
node 3 size: 258040 MB
node 3 free: 257612 MB
node distances:
  node   0   1   2   3
  0:  10  11  20  20
  1:  11  10  20  20
  2:  20  20  10  11
  3:  20  20  11  10

From /proc/meminfo
  MemTotal:       1056493796 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
  Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

(Continued on next page)
## Platform Notes (Continued)

- **CVE-2018-12207 (iTLB Multihit):** Not affected
- **CVE-2018-3620 (L1 Terminal Fault):** Not affected
- **Microarchitectural Data Sampling:** Not affected
- **CVE-2017-5754 (Meltdown):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- **CVE-2017-5715 (Spectre variant 2):** Not affected
- **CVE-2020-0543 (Special Register Buffer Data Sampling):** Not affected
- **CVE-2019-11135 (TSX Asynchronous Abort):** Not affected

---

run-level 3 Aug 16 23:48

SPEC is set to: /home/cpu2017

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<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
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<tr>
<td>/dev/sdb2</td>
<td>btrfs</td>
<td>222G</td>
<td>33G</td>
<td>189G</td>
<td>15%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

- **Vendor:** Cisco Systems Inc
- **Product:** UCSC-C220-M6S
- **Serial:** WZP244104TF

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- **Memory:**
  - 32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200

- **BIOS:**
  - **BIOS Vendor:** Cisco Systems, Inc.
  - **BIOS Version:** C220M6.4.2.1c.1.0701210708
  - **BIOS Date:** 07/01/2021
  - **BIOS Revision:** 5.22

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6326, 2.90GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6326, 2.90GHz)

SPECrate®2017_int_base = 260
SPECrate®2017_int_peak = 268

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Hardware Availability: Jun-2021
Software Availability: Dec-2020

Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C       | 502.gcc_r(peak)
-----------------------------

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
   | 525.x264_r(base, peak) 557.xz_r(base)
-----------------------------

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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C       | 500.perlbench_r(peak) 557.xz_r(peak)
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C       | 502.gcc_r(peak)
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C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6326, 2.90GHz)

Compiler Version Notes (Continued)

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C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran | 548.exchange2_r(base, peak)
-------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6326, 2.90GHz)

SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6326, 2.90GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Base Compiler Invocation

C benchmarks:
lcx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-fflto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -fflto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6326, 2.90GHz)

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</table>

**Base Optimization Flags (Continued)**

Fortran benchmarks (continued):
- -L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
- -lqkmalloc

**Peak Compiler Invocation**

C benchmarks (except as noted below):
- icx
- 500.perlbench\textunderscore r: icc
- 557.xz\textunderscore r: icc

C++ benchmarks:
- icpx

Fortran benchmarks:
- ifort

**Peak Portability Flags**

500.perlbench\textunderscore r: -DSPEC\textunderscore LP64 -DSPEC\textunderscore LINUX\textunderscore X64
502.gcc\textunderscore r: -D\_FILE\_OFFSET\_BITS=64
505.mcf\textunderscore r: -DSPEC\textunderscore LP64
520.omnetpp\textunderscore r: -DSPEC\textunderscore LP64
523.xalancbmk\textunderscore r: -DSPEC\textunderscore LP64 -DSPEC\textunderscore LINUX
525.x264\textunderscore r: -DSPEC\textunderscore LP64
531.deepsjeng\textunderscore r: -DSPEC\textunderscore LP64
541.leela\textunderscore r: -DSPEC\textunderscore LP64
548.exchange2\textunderscore r: -DSPEC\textunderscore LP64
557.xz\textunderscore r: -DSPEC\textunderscore LP64

**Peak Optimization Flags**

C benchmarks:
- 500.perlbench\textunderscore r: -Wl, -z, muldefs -prof\textunderscore gen(pass 1) -prof\textunderscore use(pass 2)
- -xCORE\textunderscore AVX512 -ipo -O3 -no\textunderscore prec\textunderscore div
- -qopt\textunderscore mem\textunderscore layout\textunderscore trans=4 -fno\textunderscore strict\textunderscore overflow
- -mbranches\textunderscore within\textunderscore 32B\textunderscore boundaries

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6326, 2.90GHz)

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Aug-2021  
**Hardware Availability:** Jun-2021  
**Tested by:** Cisco Systems  
**Software Availability:** Dec-2020

### Peak Optimization Flags (Continued)

500.perlbench_r (continued):
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`  
- `-lqkmalloc`

502.gcc_r: `-m32`
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin`  
- `-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass1)`  
- `-fprofile-use=default.profdatapass2 -xCORE-AVX512 -flto`  
- `-Ofast(pass1) -O3 -ffast-math -qopt-mem-layout-trans=4`  
- `-mbranches-within-32B-boundaries`  
- `-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc`

505.mcf_r: `basepeak = yes`

525.x264_r: `-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto`  
- `-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias`  
- `-mbranches-within-32B-boundaries`  
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`  
- `-lqkmalloc`

557.xz_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
- `-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries`  
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`  
- `-lqkmalloc`

**C++ benchmarks:**

520.omnetpp_r: `basepeak = yes`

523.xalancbmk_r: `basepeak = yes`

531.deepsjeng_r: `basepeak = yes`

541.leela_r: `basepeak = yes`

**Fortran benchmarks:**

548.exchange2_r: `basepeak = yes`

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6326, 2.90GHz)

SPECrate®2017_int_base = 260
SPECrate®2017_int_peak = 268

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

SPEC CPU®2017 Integer Rate Result
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