Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5318Y, 2.10GHz)

SPECspeed®2017_fp_base = 173
SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Threads
603.bwaves_s 48
607.cactuBSSN_s 48
619.lbm_s 48
621.wrf_s 48
627.cam4_s 48
628.pop2_s 48
638.imagick_s 48
644.nab_s 48
649.fotonik3d_s 48
654.roms_s 48

SPECspeed®2017_fp_base (173)

Hardware
CPU Name: Intel Xeon Gold 5318Y
Max MHz: 3400
Nominal: 2100
Enabled: 48 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 36 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2933)
Storage: 1 x 240GB SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
Compiler: Fortran: Version 2021.1 of Intel Fortran Compiler
Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler
Classic Build 20201112 for Linux
Parallel: Yes
Firmware: Version 4.2.1d released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
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Cisco UCS C240 M6 (Intel Xeon Gold 5318Y, 2.10GHz)

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>603.bwaves_s</td>
<td>48</td>
<td>91.9</td>
<td>642</td>
<td>92.1</td>
<td>640</td>
<td>92.5</td>
<td>638</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>48</td>
<td>76.5</td>
<td>218</td>
<td>77.0</td>
<td>216</td>
<td>78.5</td>
<td>212</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>48</td>
<td>44.6</td>
<td>117</td>
<td>41.3</td>
<td>127</td>
<td>40.5</td>
<td>129</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>48</td>
<td>97.6</td>
<td>136</td>
<td>97.7</td>
<td>135</td>
<td>98.2</td>
<td>135</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>48</td>
<td>74.7</td>
<td>119</td>
<td>75.1</td>
<td>118</td>
<td>74.9</td>
<td>118</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>48</td>
<td>161</td>
<td>73.7</td>
<td>162</td>
<td>73.5</td>
<td>162</td>
<td>73.3</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>48</td>
<td>79.5</td>
<td>181</td>
<td>78.7</td>
<td>183</td>
<td>78.8</td>
<td>183</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>48</td>
<td>60.5</td>
<td>289</td>
<td>60.5</td>
<td>289</td>
<td>60.6</td>
<td>288</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>48</td>
<td>87.8</td>
<td>104</td>
<td>87.5</td>
<td>104</td>
<td>88.1</td>
<td>103</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>48</td>
<td>73.4</td>
<td>215</td>
<td>73.5</td>
<td>214</td>
<td>73.6</td>
<td>214</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCF_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9–7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5318Y, 2.10GHz)

General Notes (Continued)

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel Hyper-Threading Technology set to Disabled
DCU Streamer Prefetch set to Disabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Processor C6 Report set to Enabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on install Mon Aug 30 16:56:08 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 5318Y CPU @ 2.10GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lscpu from util-linux 2.33.1:
  Architecture:  x86_64
  CPU op-mode(s): 32-bit, 64-bit
  Byte Order:  Little Endian

(Continued on next page)
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SPECSpeed®2017_fp_base = 173
SPECSpeed®2017_fp_peak = Not Run

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</tbody>
</table>

**Platform Notes (Continued)**

Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 1
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 5318Y CPU @ 2.10GHz
Stepping: 6
CPU MHz: 1217.593
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 36864K
NUMA node0 CPU(s): 0-23
NUMA nodel CPU(s): 24-47
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtr偶 pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibs ibbp ibrs ibrs_enhanced tpr_shadow vmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsaveopt xsaves xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfn vaes vpclmulqdq avx512_vnni avx512_vbalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

```
From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
node 0 size: 1031745 MB
node 0 free: 1031155 MB
```

(Continued on next page)
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</tbody>
</table>

Platform Notes (Continued)

- node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
- node 1 size: 1032182 MB
- node 1 free: 1031609 MB
- node distances:
  - node 0 1
  - 0: 10 20
  - 1: 20 10

From /proc/meminfo
MemTotal: 2113461580 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*

- os-release:
  - NAME="SLES"
  - VERSION="15-SP2"
  - VERSION_ID="15.2"
  - PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
  - ID="sles"
  - ID_LIKE="suse"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

- CVE-2018-12207 (iTLB Multihit): Not affected
- CVE-2018-3620 (L1 Terminal Fault): Not affected
- Microarchitectural Data Sampling: Not affected
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps barriers and __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
- CVE-2019-11135 (TSX Asynchronous Abort): Not affected

(Continued on next page)
### Platform Notes (Continued)

run-level 3 Aug 28 10:54

SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use% Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda2</td>
<td>btrfs</td>
<td>222G</td>
<td>15G</td>
<td>206G</td>
<td>7% /home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

Vendor: Cisco Systems Inc  
Product: UCSC-C240-M6SX  
Serial: WZP24440K0A

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory: 

32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2933

BIOS:  
- BIOS Vendor: Cisco Systems, Inc.  
- BIOS Version: C240M6.4.2.1d.0.0730210924  
- BIOS Date: 07/30/2021  
- BIOS Revision: 5.22  

(End of data from sysinfo program)

### Compiler Version Notes

```
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
```

```
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
C++, C, Fortran | 607.cactuBSSN_s(base)
```

```
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

(Continued on next page)
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Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran, C
603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
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Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64

(Continued on next page)
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**Base Portability Flags (Continued)**

- 621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 638.imagick_s: -DSPEC_LP64 -assume byterecl
- 644.nab_s: -DSPEC_LP64
- 649.fotonik3d_s: -DSPEC_LP64
- 654.roms_s: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:

```
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries
```

Fortran benchmarks:

```
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using both Fortran and C:

```
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using Fortran, C, and C++:

```
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

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