Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6338N, 2.20GHz)

SPECspeed®2017_fp_base = 196
SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

Threads
0 30 60 90 120 150 180 210 240 270 300 330 360 390 420 450 480 510 540 570 600 630 660 690 720 750 780 810 840

603.bwaves_s 64 246
607.cactuBSSN_s 64 121 444
619.lbm_s 64 190 143
621.wrf_s 64 79 0
627.cam4_s 64 234
628.pop2_s 64 371
638.imagick_s 64 98 2
644.nab_s 64
649.fotonik3d_s 64 243
654.roms_s 64

--- SPECspeed®2017_fp_base (196) ---

Hardware
CPU Name: Intel Xeon Gold 6338N
Max MHz: 3500
Nominal: 2200
Enabled: 64 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 48 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)
Storage: 1 x 240 GB SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
Compiler: Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
Parallel: Yes
Firmware: Version 4.2.1d released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6338N, 2.20GHz)

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SPECspeed®2017_fp_base = 196
SPECspeed®2017_fp_peak = Not Run

Test Date: Aug-2021
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Results Table

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<td>61.7</td>
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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file optio was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6338N, 2.20GHz)

SPECs\textsuperscript{2017\textsubscript{fp}}\_\textsubscript{base} = \textit{196}
SPECs\textsuperscript{2017\textsubscript{fp}}\_\textsubscript{peak} = \textit{Not Run}

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</table>

General Notes (Continued)

```
numactl --interleave=all runcpu <etc>
```
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetcher set to Disabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Processor C6 Report set to Enabled
Intel Hyper-Threading Technology set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca64d
running on localhost Mon Aug 30 05:45:53 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
```
model name : Intel(R) Xeon(R) Gold 6338N CPU @ 2.20GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 32
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
  25 26 27 28 29 30 31
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
  25 26 27 28 29 30 31
```

From lscpu from util-linux 2.33.1:

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6338N, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_fp_base = 196
SPECspeed®2017_fp_peak = Not Run

Platform Notes (Continued)

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 1
Core(s) per socket: 32
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6338N CPU @ 2.20GHz
Stepping: 6
CPU MHz: 2728.755
CPU max MHz: 3500.0000
CPU min MHz: 800.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 49152K
NUMA node0 CPU(s): 0-31
NUMA node1 CPU(s): 32-63
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmlen flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsavec xsavec xsave v镧 vcmp l cad ms xsaveopt xsaveopt xsaves cmq llc cmq_occuc llc cmq_mbm_total cmq_mbm_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vbmi umip pkt ospe avx512_vbmi2 gfi vaes vpcmldqavx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)

(Continued on next page)
Cisco Systems
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Platform Notes (Continued)

node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
28 29 30 31
node 0 size: 1031776 MB
node 0 free: 1027363 MB
node 1 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56
57 58 59 60 61 62 63
node 1 size: 1032146 MB
node 1 free: 1031388 MB
node distances:
node 0 1
0: 10 20
1: 20 10

From /proc/meminfo
MemTotal: 2113457788 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):
Not affected
CVE-2018-3620 (L1 Terminal Fault):
Not affected
Microarchitectural Data Sampling:
Not affected
CVE-2017-5754 (Meltdown):
Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass):
Mitigation: usercopy/swaps barriers and __user pointer
CVE-2017-5753 (Spectre variant 1):

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6338N, 2.20GHz)

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Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
sanitization
CVE-2020-0543 (Special Register Buffer Data Sampling):
Not affected
CVE-2019-11135 (TSX Asynchronous Abort):
Not affected

run-level 3 Aug 30 01:21
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 222G 17G 204G 8% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C240-M6S
Serial: WZP24460JDQ

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C240M6.4.2.1d.0.0730210924
BIOS Date: 07/30/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes
==============================================================================
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

C++, C, Fortran | 607.cactuBSSN_s(base)

Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6338N, 2.20GHz)

SPECspeed®2017_fp_base = 196
SPECspeed®2017_fp_peak = Not Run

Compiler Version Notes (Continued)

Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort
## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6338N, 2.20GHz)

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### Base Portability Flags

- 603.bwaves_s: `-DSPEC_LP64`
- 607.cactuBSSN_s: `-DSPEC_LP64`
- 619.ibm_s: `-DSPEC_LP64`
- 621.wrf_s: `-DSPEC_LP64` `-DSPEC_CASE_FLAG` `-convert big_endian`
- 627.cam4_s: `-DSPEC_LP64` `-DSPEC_CASE_FLAG`
- 628.pop2_s: `-DSPEC_LP64` `-DSPEC_CASE_FLAG` `-convert big_endian` `-assume byterecl`
- 638.imagick_s: `-DSPEC_LP64`
- 644.nab_s: `-DSPEC_LP64`
- 649.fotonik3d_s: `-DSPEC_LP64`
- 654.roms_s: `-DSPEC_LP64`

### Base Optimization Flags

**C benchmarks:**

- `-m64` `-std=c11` `-xCORE-AVX2` `-ipo` `-O3` `-no-prec-div` `-qopt-prefetch` `-ffinite-math-only` `-qopt-mem-layout-trans=4` `-qopenmp` `-DSPEC_OPENMP` `-mbranches-within-32B-boundaries`

**Fortran benchmarks:**

- `-m64` `-Wl,-z,muldefs` `-DSPEC_OPENMP` `-xCORE-AVX2` `-ipo` `-O3` `-no-prec-div` `-qopt-prefetch` `-ffinite-math-only` `-qopt-mem-layout-trans=4` `-qopenmp` `-nostandard-realloc-lhs` `-mbranches-within-32B-boundaries` `-L/usr/local/jemalloc64-5.0.1/lib` `-ljemalloc`

**Benchmarks using both Fortran and C:**

- `-m64` `-std=c11` `-Wl,-z,muldefs` `-xCORE-AVX2` `-ipo` `-O3` `-no-prec-div` `-qopt-prefetch` `-ffinite-math-only` `-qopt-mem-layout-trans=4` `-qopenmp` `-DSPEC_OPENMP` `-mbranches-within-32B-boundaries` `-nostandard-realloc-lhs` `-L/usr/local/jemalloc64-5.0.1/lib` `-ljemalloc`

**Benchmarks using Fortran, C, and C++:**

- `-m64` `-std=c11` `-Wl,-z,muldefs` `-xCORE-AVX2` `-ipo` `-O3` `-no-prec-div` `-qopt-prefetch` `-ffinite-math-only` `-qopt-mem-layout-trans=4` `-qopenmp` `-DSPEC_OPENMP` `-mbranches-within-32B-boundaries` `-nostandard-realloc-lhs` `-L/usr/local/jemalloc64-5.0.1/lib` `-ljemalloc`

The flags files that were used to format this result can be browsed at:

**Cisco Systems**

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You can also download the XML flags sources by saving the following links:


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Tested with SPEC CPU®2017 v1.1.8 on 2021-08-30 05:45:53-0400.


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