Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

CPU Name: Intel Xeon Silver 4309Y
Max MHz: 3600
Nominal: 2800
Enabled: 16 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
Cache L2: 1.25 MB I+D on chip per core
Cache L3: 12 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2666)
Storage: 1 x 240 GB M2 SSD
Other: None

OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
Compiler: Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
Parallel: Yes
Firmware: Version 4.2.1d released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage

SPECspeed®2017_fp_peak = Not Run
SPECspeed®2017_fp_base = 103
## SPEC CPU®2017 Floating Point Speed Result

### Cisco Systems

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### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>16</td>
<td>152</td>
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<td>152</td>
<td>387</td>
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<tr>
<td>607.cactuBSSN_s</td>
<td>16</td>
<td>134</td>
<td>124</td>
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<td>120</td>
<td>142</td>
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<tr>
<td>619.lbm_s</td>
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<td>75.5</td>
<td>69.2</td>
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<td>621.wrf_s</td>
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<td>627.cam4_s</td>
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<td>59.8</td>
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<td>628.pop2_s</td>
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<td>85.1</td>
<td>169</td>
<td>85.2</td>
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<tr>
<td>644.nab_s</td>
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<td>143</td>
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<tr>
<td>649.fotonik3d_s</td>
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<td>78.5</td>
<td>116</td>
<td>78.8</td>
<td>116</td>
<td>78.9</td>
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<tr>
<td>654.roms_s</td>
<td>16</td>
<td>165</td>
<td>95.6</td>
<td>165</td>
<td>95.5</td>
<td>165</td>
<td>95.3</td>
<td></td>
</tr>
</tbody>
</table>

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- MALLOC_CONF = "retain:true"
- OMP_STACKSIZE = "192M"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```bash
sync; echo 3 >/proc/sys/vm/drop_caches
```

Runcpu command invoked through numactl i.e.:

(Continued on next page)
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General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel Hyper-Threading Technology set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca64d
running on localhost Thu Aug 26 02:56:01 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4309Y CPU @ 2.80GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit

(Continued on next page)
Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

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<thead>
<tr>
<th>Platform Notes (Continued)</th>
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<tbody>
<tr>
<td><strong>Byte Order:</strong></td>
</tr>
<tr>
<td><strong>Address sizes:</strong></td>
</tr>
<tr>
<td><strong>CPU(s):</strong></td>
</tr>
<tr>
<td><strong>On-line CPU(s) list:</strong></td>
</tr>
<tr>
<td><strong>Thread(s) per core:</strong></td>
</tr>
<tr>
<td><strong>Core(s) per socket:</strong></td>
</tr>
<tr>
<td><strong>Socket(s):</strong></td>
</tr>
<tr>
<td><strong>NUMA node(s):</strong></td>
</tr>
<tr>
<td><strong>Vendor ID:</strong></td>
</tr>
<tr>
<td><strong>CPU family:</strong></td>
</tr>
<tr>
<td><strong>Model:</strong></td>
</tr>
<tr>
<td><strong>Model name:</strong></td>
</tr>
<tr>
<td><strong>Stepping:</strong></td>
</tr>
<tr>
<td><strong>CPU MHz:</strong></td>
</tr>
<tr>
<td><strong>CPU max MHz:</strong></td>
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<tr>
<td><strong>CPU min MHz:</strong></td>
</tr>
<tr>
<td><strong>BogoMIPS:</strong></td>
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<tr>
<td><strong>Virtualization:</strong></td>
</tr>
<tr>
<td><strong>L1d cache:</strong></td>
</tr>
<tr>
<td><strong>L1i cache:</strong></td>
</tr>
<tr>
<td><strong>L2 cache:</strong></td>
</tr>
<tr>
<td><strong>L3 cache:</strong></td>
</tr>
<tr>
<td><strong>NUMA node0 CPU(s):</strong></td>
</tr>
<tr>
<td><strong>NUMA node1 CPU(s):</strong></td>
</tr>
<tr>
<td><strong>Flags:</strong></td>
</tr>
<tr>
<td><strong>/proc/cpuinfo cache data</strong></td>
</tr>
<tr>
<td>cache size : 12288 KB</td>
</tr>
</tbody>
</table>

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7
node 0 size: 1031782 MB

(Continued on next page)
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SPECspeed®2017_fp_base = 103
SPECspeed®2017_fp_peak = Not Run

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

node 0 free: 1028553 MB
node 1 cpus: 8 9 10 11 12 13 14 15
node 1 size: 1032152 MB
node 1 free: 1030358 MB
node distances:
node  0  1
0:  10  20
1:  20  10

From /proc/meminfo
MemTotal:     2113469064 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5753 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2017-5715 (Spectre variant 2): Not affected
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected

(Continued on next page)
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SPECspeed®2017_fp_base = 103
SPECspeed®2017_fp_peak = Not Run

Platform Notes (Continued)

CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Aug 25 20:32

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 222G 17G 204G 8% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C240-M6S
Serial: WZP24460JDQ

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C240M6.4.2.1d.0.0730210924
BIOS Date: 07/30/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

-----------------------------------------------------------------------------------
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
-----------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------------

-----------------------------------------------------------------------------------
C++, C, Fortran | 607.cactuBSSN_s(base)
-----------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
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**Compiler Version Notes (Continued)**

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) Fortran Intel (R) 64 Compiler Classic for applications running on
Intel (R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
```

Intel (R) Fortran Intel (R) 64 Compiler Classic for applications running on
Intel (R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
Base Compiler Invocation
```

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

```
Base Portability Flags
```

603.bwaves_s: -DSPEC_LP64
607.cactusSNS_s: -DSPEC_LP64

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### Base Portability Flags (Continued)

619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

### Base Optimization Flags

C benchmarks:
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries

Fortran benchmarks:
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both Fortran and C:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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