Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4310T, 2.30GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 144</th>
<th>SPECrate®2017_int_peak = 148</th>
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<tr>
<td>CPU2017 License: 9019</td>
<td>Test Date: Sep-2021</td>
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<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2021</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Dec-2020</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Silver 4310T
- **Max MHz:** 3400
- **Nominal:** 2300
- **Enabled:** 20 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **Cache L2:** 1.25 MB I+D on chip per core
- **Cache L3:** 15 MB I+D on chip per chip
- **Other:** None
- **Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2666)
- **Storage:** 1 x 240 GB M.2 SSD SATA
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
- **Parallel:** No
- **Firmware:** Version 4.2.1d released Jul-2021
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage

### SPEC CPU®2017 Integer Rate Result

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#### Table of Results

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<tr>
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<td>omnetpp_r</td>
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<td>xalancbmk_r</td>
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<td>xz_r</td>
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## Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4310T, 2.30GHz)

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<td>mcf_r</td>
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<td>omnetpp_r</td>
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<td>95.1</td>
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<td>80.2</td>
<td>540</td>
<td>80.0</td>
<td>539</td>
<td>80.2</td>
</tr>
</tbody>
</table>

### Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes
Environment variables set by runcpu before the start of the run:

```bash
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"
```

### General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesysten page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

SPECrate®2017_int_base = 144
SPECrate®2017_int_peak = 148

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
<thead>
<tr>
<th>General Notes (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>numactl --interleave=all runcpu &lt;etc&gt;</td>
</tr>
<tr>
<td>NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.</td>
</tr>
<tr>
<td>Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.</td>
</tr>
<tr>
<td>Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Platform Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIOS Settings:</td>
</tr>
<tr>
<td>Adjacent Cache Line Prefetcher set to Disabled</td>
</tr>
<tr>
<td>DCU Streamer Prefetch set to Disabled</td>
</tr>
<tr>
<td>UPI Link Enablement set to 1</td>
</tr>
<tr>
<td>UPI Power Management set to Enabled</td>
</tr>
<tr>
<td>Sub NUMA Clustering set to Enabled</td>
</tr>
<tr>
<td>LLC Dead Line set to Disabled</td>
</tr>
<tr>
<td>Memory Refresh Rate set to 1x Refresh</td>
</tr>
<tr>
<td>ADDDC Sparing set to Disabled</td>
</tr>
<tr>
<td>Patrol Scrub set to Disabled</td>
</tr>
<tr>
<td>Energy Efficient Turbo set to Enabled</td>
</tr>
<tr>
<td>Processor C6 Report set to Enabled</td>
</tr>
<tr>
<td>Processor C1E set to Enabled</td>
</tr>
<tr>
<td>Sysinfo program /home/cpu2017/bin/sysinfo</td>
</tr>
<tr>
<td>Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acac64d running on localhost Wed Sep 1 04:25:46 2021</td>
</tr>
</tbody>
</table>

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4310T CPU @ 2.30GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 5 6 7 8 9
physical 1: cores 0 1 2 3 4 5 6 7 8 9

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPECrate®2017_int_base = 144
SPECrate®2017_int_peak = 148

Platform Notes (Continued)

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4310T CPU @ 2.30GHz
Stepping: 6
CPU MHz: 2021.760
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 15360K
NUMA node0 CPU(s): 0-9,20-29
NUMA node1 CPU(s): 10-19,30-39
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpre pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abtm 3dnowprefetch cpuid_fault ebpx cat_13 invvpica single ssbd mba ibrs ibbp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpd ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3dnow invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma cmclflushopt clwb intel_pt avx512cd sha_ni
avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsavec lgcm_llc lgcm_occup_llc lgcm_mbm_total
lgcm_mbm_local lbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512v bmi umip pku ospe avx512_vbmi2 gfnl vspec vpcmulqdq avx512_vnni
avx512_bitalg tme avx512_vpoptnqd 1a57 rdpid md_clear pconfig flush_lld
arch_capabilities

From numactl --hardware
CACHE size : 15360 KB

WARNING: a numactl 'node' might or might not correspond to a physical chip.
Platform Notes (Continued)

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
node 0 size: 1031594 MB
node 0 free: 1031073 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
node 1 size: 1031873 MB
node 1 free: 1031342 MB

node distances:
node 0: 10 20
node 1: 20 10

From /proc/meminfo
MemTotal: 2112944812 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4310T, 2.30GHz)

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Test Date: Sep-2021
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Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Sep 1 04:19
SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 222G 9.1G 212G 5% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH24097576

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is"intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
  BIOS Vendor: Cisco Systems, Inc.
  BIOS Version: B200M6.4.2.1d.0.0730210924
  BIOS Date: 07/30/2021
  BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 500.perlbench_r(peak) 557.xz_r(peak)
==============================================================================

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C       | 502.gcc_r(peak)
==============================================================================

Intel(R) oneAPI DPC+/C++ Compiler for applications running on IA-32, Version
2021.1 Build 20201113

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4310T, 2.30GHz)

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**Compiler Version Notes (Continued)**

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

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C       | 500.perlbench_r(peak) 557.xz_r(peak)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
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```

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C       | 502.gcc_r(peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
2021.1 Build 20201113
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```

```
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
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C       | 502.gcc_r(peak)
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Compiler Version Notes (Continued)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
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C benchmarks
- 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
- 525.x264_r(base, peak) 557.xz_r(base)

C++ benchmarks
- 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
- 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Fortran benchmarks
- 548.exchange2_r(base, peak)

Base Compiler Invocation

C benchmarks:
- icx

C++ benchmarks:
- icpx

Fortran benchmarks:
- ifort
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPEC CPU®2017 Integer Rate Result
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Base Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L[opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation
C benchmarks (except as noted below):
icx

500.perlbench_r: icx

(Continued on next page)
## Peak Compiler Invocation (Continued)

557.xz_r: icc

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

## Peak Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>-D_FILE_OFFSET_BITS=64</td>
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<tr>
<td>505.mcf_r</td>
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<td>520.omnetpp_r</td>
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<td>541.leela_r</td>
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<td>548.exchange2_r</td>
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<tr>
<td>557.xz_r</td>
<td>-DSPEC_LP64</td>
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</table>

## Peak Optimization Flags

### C benchmarks:

500.perlbench_r:
- Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
- -xCORE-AVX512 -ipo -03 -no-prec-div
- -qopt-mem-layout-trans=4 -fno-strict-overflow
- -mbranches-within-32B-boundaries
- -L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
- -lqkmalloc

502.gcc_r:
- -m32
- -L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
- -std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
- -fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
- -Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
- -mbranches-within-32B-boundaries
- -L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r:
- basepeak = yes

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Silver 4310T, 2.30GHz)

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**Peak Optimization Flags (Continued)**

```bash
525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -gopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-1qkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-gopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-1qkmalloc
```

C++ benchmarks:

- 520.omnetpp_r: basepeak = yes
- 523.xalancbmk_r: basepeak = yes
- 531.deepsjeng_r: basepeak = yes
- 541.leela_r: basepeak = yes

Fortran benchmarks:

- 548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-09-01 07:25:45-0400.
Report generated on 2021-09-29 12:24:50 by CPU2017 PDF formatter v6442.
Originally published on 2021-09-28.