SPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)

SPECspeed®2017_fp_base = 119
SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Threads

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>24</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>24</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>24</td>
</tr>
<tr>
<td>621.wrf_s</td>
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</tr>
<tr>
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</tr>
<tr>
<td>644.nab_s</td>
<td>24</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>24</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>24</td>
</tr>
</tbody>
</table>

Hardware

CPU Name: Intel Xeon Gold 6312U
Max MHz: 3600
Nominal: 2400
Enabled: 24 cores, 1 chip
Orderable: 1 Chip
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 36 MB I+D on chip per chip
Other: None
Memory: 512 GB (8 x 64 GB 2Rx4 PC4-3200V-R)
Storage: 1 x 240 GB M.2 SSD SATA
Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP2
Compiler: Fortran: Version 2021.1 of Intel Fortran Compiler
          Classic Build 20201112 for Linux;
          C/C++: Version 2021.1 of Intel C/C++ Compiler
          Classic Build 20201112 for Linux

Firmware: Version 4.2.1d released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
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Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Results Table

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<tr>
<th>Benchmark</th>
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<th>Seconds</th>
<th>Ratio</th>
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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
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Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)

SPECspeed®2017_fp_base = 119
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel Hyper-Threading Technology set to Disabled
DCU Streamer Prefetch set to Disabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on localhost Thu Sep  9 18:28:02 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6312U CPU @ 2.40GHz
  1 "physical id"s (chips)
  24 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From /proc/cpuinfo
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian

(Continued on next page)
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Sep-2021  
**Hardware Availability:** Apr-2021  
**Tested by:** Cisco Systems  
**Software Availability:** Dec-2020

### Platform Notes (Continued)

- **Address sizes:** 46 bits physical, 57 bits virtual  
- **CPU(s):** 24  
- **On-line CPU(s) list:** 0-23  
- **Thread(s) per core:** 1  
- **Core(s) per socket:** 24  
- **Socket(s):** 1  
- **NUMA node(s):** 1  
- **Vendor ID:** GenuineIntel  
- **CPU family:** 6  
- **Model:** 106  
- **Model name:** Intel(R) Xeon(R) Gold 6312U CPU @ 2.40GHz  
- **Stepping:** 6  
- **CPU MHz:** 850.741  
- **CPU max MHz:** 3600.0000  
- **CPU min MHz:** 800.0000  
- **BogoMIPS:** 4800.00  
- **Virtualization:** VT-x  
- **L1d cache:** 48K  
- **L1i cache:** 32K  
- **L2 cache:** 1280K  
- **L3 cache:** 36864K  
- **NUMA node0 CPU(s):** 0-23  
- **Flags:** fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enabled tpr_shadow vmi fpxrc vpxtd fault_ad ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3dnow invvdpc rtm cqm rdt_a avx512f avx512dq rdseedadx smap avx512fma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsavevc xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vnni umip pku ospke avx512_vbmi2 gfnv vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_lid arch_capabilities

From numactl --hardware  
**WARNING:** a numactl 'node' might or might not correspond to a physical chip.  
**available:** 1 nodes (0)  
**node 0 cpus:** 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23  
**node 0 size:** 515107 MB  
**node 0 free:** 507377 MB  
**node distances:**

(Continued on next page)
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SPECTM2017_fp_base = 119
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Platform Notes (Continued)

node 0
0: 10

From /proc/meminfo
MemTotal: 527469992 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swaps barriers and __user pointer sanitation
CVE-2017-5753 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2017-5715 (Spectre variant 2):
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Sep 9 14:24
SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on

(Continued on next page)
## Platform Notes (Continued)

```
/dev/sda2  btrfs  222G  15G  206G  7% /home
```

From /sys/devices/virtual/dmi/id
- **Vendor:** Cisco Systems Inc
- **Product:** UCSB-B200-M6
- **Serial:** FCH24097576

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- **Memory:**
  - 8x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200
  - 24x NO DIMM NO DIMM

- **BIOS:**
  - **Vendor:** Cisco Systems, Inc.
  - **Version:** B200M6.4.2.1d.0.0730210924
  - **Date:** 07/30/2021
  - **Revision:** 5.22

(End of data from sysinfo program)

## Compiler Version Notes

```
C                | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
```

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
C++, C, Fortran   | 607.cactuBSSN_s(base)
```

Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

(Continued on next page)
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Compiler Version Notes (Continued)

Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran, C      | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
  icc

Fortran benchmarks:
  ifort

Benchmarks using both Fortran and C:
  ifort icc

Benchmarks using Fortran, C, and C++:
  icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
  -assume byteordered
## Cisco Systems

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### Base Portability Flags (Continued)

- `638.imagick_s`: -DSPEC_LP64
- `644.nab_s`: -DSPEC_LP64
- `649.fotonik3d_s`: -DSPEC_LP64
- `654.roms_s`: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**

```
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries
```

**Fortran benchmarks:**

```
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

**Benchmarks using both Fortran and C:**

```
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
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The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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