SPEC CPU®2017 Integer Rate Result

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Cisco Systems

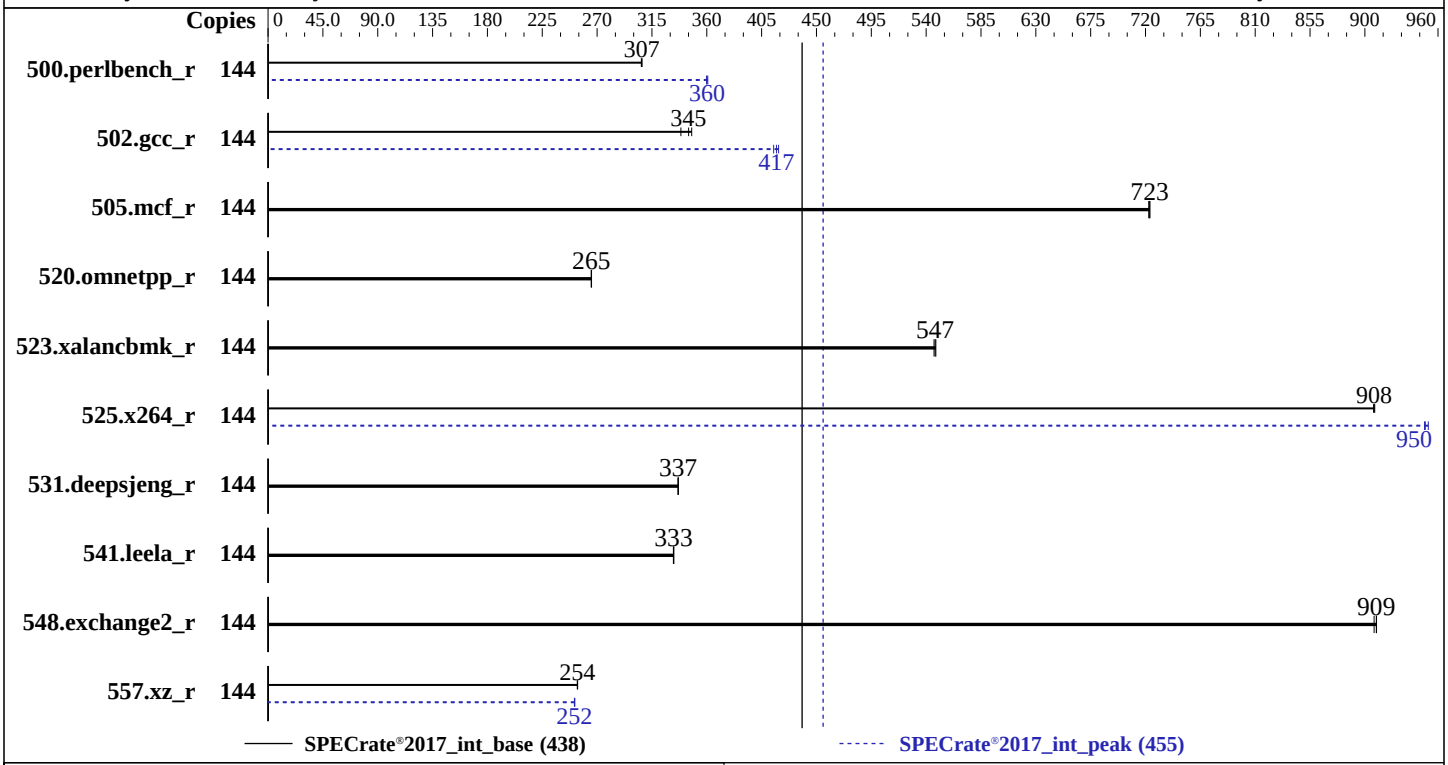
Cisco UCS C240 M6 (Intel Xeon Platinum 8352V, 2.10GHz)

SPECrate®2017_int_base = 438

SPECrate®2017_int_peak = 455

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020



Hardware

CPU Name:	Intel Xeon Platinum 8352V
Max MHz:	3500
Nominal:	2100
Enabled:	72 cores, 2 chips, 2 threads/core
Orderable:	1,2 Chips
Cache L1:	32 KB I + 48 KB D on chip per core
L2:	1.25 MB I+D on chip per core
L3:	54 MB I+D on chip per chip
Other:	None
Memory:	2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2933)
Storage:	1 x 960 GB M.2 SSD SATA
Other:	None

Software

OS:	SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
Compiler:	C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
Parallel:	No
Firmware:	Version 4.2.1d released Jul-2021
File System:	btrfs
System State:	Run level 3 (multi-user)
Base Pointers:	64-bit
Peak Pointers:	32/64-bit
Other:	jemalloc memory allocator V5.0.1
Power Management:	BIOS and OS set to prefer performance at the cost of additional power usage

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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	144	747	307	**747**	**307**	748	306	144	637	360	635	361	**636**	**360**
502.gcc_r	144	**591**	**345**	587	348	602	339	144	491	415	487	419	**489**	**417**
505.mcf_r	144	322	723	322	724	**322**	**723**	144	322	723	322	724	**322**	**723**
520.omnetpp_r	144	**712**	**265**	712	265	712	265	144	**712**	**265**	712	265	712	265
523.xalancbmk_r	144	278	546	**278**	**547**	278	548	144	278	546	**278**	**547**	278	548
525.x264_r	144	**278**	**908**	278	907	278	908	144	266	949	265	952	**266**	**950**
531.deepsjeng_r	144	490	337	490	336	**490**	**337**	144	490	337	490	336	**490**	**337**
541.leela_r	144	**716**	**333**	717	333	716	333	144	**716**	**333**	717	333	716	333
548.exchange2_r	144	416	908	415	910	**415**	**909**	144	416	908	415	910	**415**	**909**
557.xz_r	144	**612**	**254**	613	254	612	254	144	618	252	619	251	**618**	**252**

SPECrate®2017_int_base = 438

SPECrate®2017_int_peak = 455

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

```
The numactl mechanism was used to bind copies to processors. The config file option 'submit'
was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.
```

Operating System Notes

```
 Stack size set to unlimited using "ulimit -s unlimited"
cpupower frequency-set -g performance run as root to set the scaling governor to
performance.
```

Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
     "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-
     32"
MALLOC_CONF = "retain:true"
```

General Notes

```
 Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
 memory using openSUSE Leap 15.2
 Transparent Huge Pages enabled by default
 Prior to runcpu invocation
```

(Continued on next page)

General Notes (Continued)

```
 Filesystem page cache synced and cleared with:
 sync; echo 3>       /proc/sys/vm/drop_caches
 runcpu command invoked through numactl i.e.:
 numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases
```

Platform Notes

```
BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Processor C6 Report set to Enabled
Processor C1E set to Enabled

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
 running on install Fri Sep 24 15:31:58 2021

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Platinum 8352V CPU @ 2.10GHz
       2  "physical id"s (chips)
       144 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 36
       siblings  : 72
```

(Continued on next page)

Platform Notes (Continued)

```
      physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
      25 26 27 28 29 30 31 32 33 34 35
      physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
      25 26 27 28 29 30 31 32 33 34 35

 From lscpu from util-linux 2.33.1:
      Architecture:        x86_64
      CPU op-mode(s):      32-bit, 64-bit
      Byte Order:          Little Endian
      Address sizes:       46 bits physical, 57 bits virtual
      CPU(s):              144
      On-line CPU(s) list: 0-143
      Thread(s) per core:  2
      Core(s) per socket:  36
      Socket(s):           2
      NUMA node(s):        4
      Vendor ID:           GenuineIntel
      CPU family:          6
      Model:               106
      Model name:          Intel(R) Xeon(R) Platinum 8352V CPU @ 2.10GHz
      Stepping:            6
      CPU MHz:             2969.774
      CPU max MHz:         3500.0000
      CPU min MHz:         800.0000
      BogoMIPS:            4200.00
      Virtualization:      VT-x
      L1d cache:           48K
      L1i cache:           32K
      L2 cache:            1280K
      L3 cache:            55296K
      NUMA node0 CPU(s):   0-17,72-89
      NUMA node1 CPU(s):   18-35,90-107
      NUMA node2 CPU(s):   36-53,108-125
      NUMA node3 CPU(s):   54-71,126-143
      Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
      pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
      lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
      aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
      xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
      avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
      mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
      fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
      avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni
      avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
      cqm_mbm_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
      hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni
      avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
```

(Continued on next page)

Platform Notes (Continued)

```
      arch_capabilities

 /proc/cpuinfo cache data
    cache size : 55296 KB

 From numactl --hardware
 WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 4 nodes (0-3)
   node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 72 73 74 75 76 77 78 79 80 81
   82 83 84 85 86 87 88 89
   node 0 size: 515680 MB
   node 0 free: 515029 MB
   node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 90 91 92 93 94 95 96
   97 98 99 100 101 102 103 104 105 106 107
   node 1 size: 516087 MB
   node 1 free: 515526 MB
   node 2 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 108 109 110 111 112
   113 114 115 116 117 118 119 120 121 122 123 124 125
   node 2 size: 516053 MB
   node 2 free: 515758 MB
   node 3 cpus: 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 126 127 128 129 130
   131 132 133 134 135 136 137 138 139 140 141 142 143
   node 3 size: 516083 MB
   node 3 free: 515799 MB
   node distances:
   node   0   1   2   3
     0:  10  11  20  20
     1:  11  10  20  20
     2:  20  20  10  11
     3:  20  20  11  10

 From /proc/meminfo
    MemTotal:       2113438460 kB
    HugePages_Total:       0
    Hugepagesize:       2048 kB

 /sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
    performance

 From /etc/*release* /etc/*version*
    os-release:
       NAME="SLES"
       VERSION="15-SP2"
       VERSION_ID="15.2"
       PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
       ID="sles"
       ID_LIKE="suse"
```

(Continued on next page)

Platform Notes (Continued)

```
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
   Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
   x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):                          Not affected
CVE-2018-3620 (L1 Terminal Fault):                       Not affected
Microarchitectural Data Sampling:                        Not affected
CVE-2017-5754 (Meltdown):                                Not affected
CVE-2018-3639 (Speculative Store Bypass):                Mitigation: Speculative Store
                                                         Bypass disabled via prctl and
                                                         seccomp
CVE-2017-5753 (Spectre variant 1):                       Mitigation: usercopy/swapgs
                                                         barriers and __user pointer
                                                         sanitization
CVE-2017-5715 (Spectre variant 2):                      Mitigation: Enhanced IBRS, IBPB:
                                                         conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):                 Not affected

run-level 3 Sep 24 15:28

SPEC is set to: /home/cpu2017
   Filesystem     Type   Size  Used Avail Use% Mounted on
   /dev/sdc2      btrfs  277G   26G  250G  10% /home

From /sys/devices/virtual/dmi/id
    Vendor:          Cisco Systems Inc
    Product:         UCSC-C240-M6SX
    Serial:          WZP244208SJ

Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  Memory:
    32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2933

BIOS:
   BIOS Vendor:       Cisco Systems, Inc.
   BIOS Version:      C240M6.4.2.1d.0.0730210924
   BIOS Date:         07/30/2021
   BIOS Revision:     5.22
```

(Continued on next page)

Platform Notes (Continued)

```
 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C       | 500.perlbench_r(peak) 557.xz_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
  2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(peak) 557.xz_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
  2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
```


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Compiler Version Notes (Continued)

```
==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(peak) 557.xz_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
  2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
        | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
```

(Continued on next page)

Compiler Version Notes (Continued)

```
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries

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Base Optimization Flags (Continued)

C++ benchmarks (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icx

500.perlbench_r: icc

557.xz_r: icc

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: `-Wl,-z,muldefs -prof-gen`(pass 1) `-prof-use`(pass 2)
`-xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=4 -fno-strict-overflow`
`-mbranches-within-32B-boundaries`
`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
`-lqkmalloc`

502.gcc_r: `-m32`
`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin`
`-std=gnu89 -Wl,-z,muldefs -fprofile-generate`(pass 1)
`-fprofile-use=default.profdata`(pass 2) `-xCORE-AVX512 -flto`
`-Ofast`(pass 1) `-O3 -ffast-math -qopt-mem-layout-trans=4`
`-mbranches-within-32B-boundaries`
`-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc`

505.mcf_r: `basepeak = yes`

525.x264_r: `-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto`
`-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias`
`-mbranches-within-32B-boundaries`
`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
`-lqkmalloc`

557.xz_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
`-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries`
`-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
`-lqkmalloc`

C++ benchmarks:

520.omnetpp_r: `basepeak = yes`

523.xalancbmk_r: `basepeak = yes`

531.deepsjeng_r: `basepeak = yes`

541.leela_r: `basepeak = yes`

Fortran benchmarks:

548.exchange2_r: `basepeak = yes`

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revJ.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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