Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6338, 2.00GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Threads

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
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</thead>
<tbody>
<tr>
<td>206</td>
<td>207</td>
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</table>

603.bwaves_s 64 248
607.cactuBSSN_s 64 137
619.lbm_s 64 187
621.wrf_s 64 189
627.cam4_s 64 149
628.pop2_s 64 80.6
638.imagick_s 64 227
644.nab_s 64 356
649.fotonik3d_s 64 113
654.roms_s 64 269

SPECspeed®2017_fp_base (206) —— SPECspeed®2017_fp_peak (207)

**Hardware**

CPU Name: Intel Xeon Gold 6338
Max MHz: 3200
Nominal: 2000
Enabled: 64 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 48 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
Storage: 1 x 240 GB M.2 SSD SATA
Other: None

**Software**

OS: SUSE Linux Enterprise Server 15 SP3 5.3.18-57-default
Compiler: C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++ Compiler Build 20210924 for Linux;
Fortran: Version 2021.4.0 of Intel Fortran Classic Build 20210910 for Linux;
C/C++: Version 2021.4.0 of Intel C/C++ Compiler Classic Build 20210910 for Linux;

Parallel: Yes
Firmware: Version 5.0.1d released Aug-2021
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<tr>
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</tr>
</tbody>
</table>

SPECspeed®2017_fp_base = 206
SPECspeed®2017_fp_peak = 207

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/intel/tbb/2021.4.0/env/./lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/libfabric/lib:/home/intel/mpi/2021.4.0/lib/release:/home/intel/mpi/2021.4.0/lib:/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin:/home/intel/compiler/2021.4.0/linux/lib:/home/intel/clck/2021.4.0/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6338, 2.00GHz)

SPECspeed®2017_fp_base = 206
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General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDCS Sparing set to Disabled
Patrol Scrub set to Disabled
Intel Hyper-Threading Technology set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acac64d
running on perf-blade1 Sun Nov 28 23:07:39 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6338 CPU @ 2.00GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 32
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27 28 29 30 31
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27 28 29 30 31

From lscpu from util-linux 2.36.2:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s):

(Continued on next page)
Platform Notes (Continued)

On-line CPU(s) list: 0-63
Thread(s) per core: 1
Core(s) per socket: 32
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6338 CPU @ 2.00GHz
Stepping: 6
CPU MHz: 1219.654
CPU max MHz: 3200.0000
CPU min MHz: 800.0000
BogoMIPS: 4000.00
Virtualization: VT-x
L1d cache: 3 MiB
L1i cache: 2 MiB
L2 cache: 80 MiB
L3 cache: 96 MiB
NUMA node0 CPU(s): 0-31
NUMA nodel CPU(s): 32-63
Vulnerability Itlb multihit: Not affected
Vulnerability L1f: Not affected
Vulnerability Mds: Not affected
Vulnerability Meltdown: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitation
Vulnerability Spectre v2: Mitigation; Enhanced IBRS, IBPB conditional, RSB filling
Vulnerability Srbds: Not affected
Vulnerability Tx s async abort: Not affected
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdtpe0size mxrart arch_perfmon pebs bts rep_good nopl xtopology nonstop-tsc pni pclmulqdq dts stles64 monitor dse _cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat _l3 invvpicid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsavesopt xsaves xsaveopt xsavec xgetbv1 xsaves cgsm_llc cgsm_mbb_total cgsm_mbb_local split_lock_detect wnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512v bmi umip pku ospke avx512_vm bmi2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid fsrmd md_clear pconfig flush_l1d arch_capabilities

(Continued on next page)
## Cisco Systems

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| SPECspeed\(^\circ\)2017 fp_base | 206 |
| SPECspeed\(^\circ\)2017 fp_peak | 207 |

| CPU2017 License: | 9019 |
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### Platform Notes (Continued)

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<tr>
<th>NAME</th>
<th>ONE-SIZE</th>
<th>ALL-SIZE</th>
<th>WAYS</th>
<th>TYPE</th>
<th>LEVEL</th>
<th>SETS</th>
<th>PHY-LINE</th>
<th>COHERENCY-SIZE</th>
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<td>64</td>
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<td>2M</td>
<td>8</td>
<td>Instruction</td>
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<td>64</td>
<td>1</td>
<td>64</td>
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<td>80M</td>
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<td>Unified</td>
<td>2</td>
<td>1024</td>
<td>1</td>
<td>64</td>
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<tr>
<td>L3</td>
<td>48M</td>
<td>96M</td>
<td>12</td>
<td>Unified</td>
<td>3</td>
<td>65536</td>
<td>1</td>
<td>64</td>
</tr>
</tbody>
</table>

From `lscpu --cache`:
```
NAME ONE-SIZE ALL-SIZE WAYS TYPE LEVEL SETS PHY-LINE COHERENCY-SIZE
L1d 48K 3M 12 Data 1 64 1 64
L1i 32K 2M 8 Instruction 1 64 1 64
L2 1.3M 80M 20 Unified 2 1024 1 64
L3 48M 96M 12 Unified 3 65536 1 64
```

From `/proc/cpuinfo cache data`:
```
cache size : 49152 KB
```

From `numactl --hardware`:
```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 0 size: 1031743 MB
node 0 free: 1030663 MB
node 1 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
node 1 size: 1032180 MB
node 1 free: 1031445 MB
node distances:
node 0 1
0: 10 20
1: 20 10
```

From `/proc/meminfo`:
```
MemTotal: 2113458424 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

From `/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor`:
```
has performance
```

From `/etc/*release*`:
```
NAME="SLES"
VERSION="15-SP3"
VERSION_ID="15.3"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp3"
```

```
uname -a:
```

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SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

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Platform Notes (Continued)

Linux perf-blade1 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5753 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2017-5715 (Spectre variant 2): Not affected
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Nov 24 21:13

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda3 xfs 181G 52G 130G 29% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSX-210C-M6
Serial: FCH25057AMV

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: X210M6.5.0.1d.0.0816211754
BIOS Date: 08/16/2021
BIOS Revision: 5.22

(End of data from sysinfo program)
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Compiler Version Notes
==============================================================================
| C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak) 644.nab_s(base) |
==============================================================================
| Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) |
| 64, Version 2021.4.0 Build 20210910_000000 |
| Copyright (C) 1985-2021 Intel Corporation. All rights reserved. |
==============================================================================
| C               | 644.nab_s(peak) |
==============================================================================
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, |
| Version 2021.4.0 Build 20210924 |
| Copyright (C) 1985-2021 Intel Corporation. All rights reserved. |
==============================================================================
| C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak) 644.nab_s(base) |
==============================================================================
| Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) |
| 64, Version 2021.4.0 Build 20210910_000000 |
| Copyright (C) 1985-2021 Intel Corporation. All rights reserved. |
==============================================================================
| C               | 644.nab_s(peak) |
==============================================================================
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, |
| Version 2021.4.0 Build 20210924 |
| Copyright (C) 1985-2021 Intel Corporation. All rights reserved. |
==============================================================================
| C++, C, Fortran | 607.cactuBSSN_s(base, peak) |
==============================================================================
| Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, |
| Version 2021.4.0 Build 20210910_000000 |
| Copyright (C) 1985-2021 Intel Corporation. All rights reserved. |
| Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, |
| Version 2021.4.0 Build 20210910_000000 |
| Copyright (C) 1985-2021 Intel Corporation. All rights reserved. |
| Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, |
| Version 2021.4.0 Build 20210910_000000 |
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Compiler Version Notes (Continued)

Fortran | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
        | 654.roms_s(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

Fortran, C | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
            | 628.pop2_s(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG

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<td>Sep-2021</td>
<td>Sep-2021</td>
</tr>
</tbody>
</table>

Test Sponsor: Cisco Systems
Tested by: Cisco Systems

**Base Portability Flags (Continued)**

628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

**Base Optimization Flags**

**C benchmarks:**
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries

**Fortran benchmarks:**
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs -mbranches-within-32B-boundaries
-L/home/cpu2017/je5.0.1-64 -ljemalloc

**Benchmarks using Fortran, C, and C++:**
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/home/cpu2017/je5.0.1-64 -ljemalloc

**Peak Compiler Invocation**

**C benchmarks (except as noted below):**
icc

644.nab_s: icx

**Fortran benchmarks:**
ifort

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6338, 2.00GHz)

SPECspeed®2017_fp_base = 206
SPECspeed®2017_fp_peak = 207

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Peak Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

619.lbm_s: basepeak = yes
638.imagick_s: basepeak = yes

644.nab_s: -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -fopenmp
-DSPEC_OPENMP -qopt-mem-layout-trans=4
-fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries -L/home/cpu2017/je5.0.1-64
-ljemalloc

Fortran benchmarks:

603.bwaves_s: -m64 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -ipo -xCORE-AVX2
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -gopenmp -nostandard-realloc-lhs
-mbranches-within-32B-boundaries -L/home/cpu2017/je5.0.1-64
-ljemalloc

649.fotonik3d_s: Same as 603.bwaves_s
654.roms_s: basepeak = yes

Benchmarks using both Fortran and C:

621.wrf_s: -m64 -std=c11 -Wl,-z,muldefs -prof-gen(pass 1)
-prof-use(pass 2) -ipo -xCORE-AVX2 -03 -no-prec-div

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6338, 2.00GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Specspeed®2017_fp_base = 206
Specspeed®2017_fp_peak = 207

Test Date: Nov-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Peak Optimization Flags (Continued)

621.wrf_s (continued):
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/home/cpu2017/je5.0.1-64 -ljemalloc

627.cam4_s: basepeak = yes
628.pop2_s: basepeak = yes

Benchmarks using Fortran, C, and C++:
607.cactuBSSN_s: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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