Cisco Systems

Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)

**SPECrater 2017_int_base** = 126

**SPECrater 2017_int_peak** = 130

<table>
<thead>
<tr>
<th>Software</th>
<th>OS: SUSE Linux Enterprise Server 15 SP3 (x86_64) kernel version 5.3.18-57-default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler:</td>
<td>C/C++/Fortran: Version 3.0.0 of AOCC</td>
</tr>
<tr>
<td>Parallel:</td>
<td>No</td>
</tr>
<tr>
<td>Firmware:</td>
<td>Version 4.2.1c released Aug-2021</td>
</tr>
<tr>
<td>File System:</td>
<td>xfs</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Other:</td>
<td>jemalloc: jemalloc memory allocator library v5.1.0</td>
</tr>
<tr>
<td>Power Management:</td>
<td>BIOS and OS set to prefer performance at the cost of additional power usage</td>
</tr>
</tbody>
</table>

**Hardware**

CPU Name: AMD EPYC 7252
Max MHz: 3200
Nominal: 3100
Enabled: 16 cores, 2 chips, 2 threads/core
Orderable: 1.2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 512 KB I+D on chip per core
L3: 64 MB I+D on chip per chip, 16 MB shared / 2 cores
Other: None
Memory: 2 TB (16 x 128 GB 4Rx4 PC4-3200V-L)
Storage: 1 x 960 GB M.2 SSD SATA
Other: None

<table>
<thead>
<tr>
<th>Copies</th>
<th>500.perlbench_r</th>
<th>502.gcc_r</th>
<th>505.mcf_r</th>
<th>520.omnetpp_r</th>
<th>523.xalancbmk_r</th>
<th>525.x264_r</th>
<th>531.deepsjeng_r</th>
<th>541.leela_r</th>
<th>548.exchange2_r</th>
<th>557.xz_r</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>87.3</td>
<td>115</td>
<td>134</td>
<td>201</td>
<td>148</td>
<td>162</td>
<td>262</td>
<td>289</td>
<td>72.1</td>
<td>72.3</td>
</tr>
</tbody>
</table>

**Test Sponsor:** Cisco Systems
**Test Date:** Nov-2021
**Hardware Availability:** Jun-2021
**Tested by:** Cisco Systems
**Software Availability:** Jun-2021
SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)

SPECrate®2017_int_base = 126
SPECrate®2017_int_peak = 130

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2021
Hardware Availability: Jun-2021
Tested by: Cisco Systems
Software Availability: Jun-2021

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>32</td>
<td>609</td>
<td>83.7</td>
<td>610</td>
<td>83.5</td>
<td>610</td>
<td>83.5</td>
<td>32</td>
<td>584</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>32</td>
<td>396</td>
<td>115</td>
<td>395</td>
<td>115</td>
<td>395</td>
<td>115</td>
<td>32</td>
<td>337</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>32</td>
<td>256</td>
<td>202</td>
<td>257</td>
<td>201</td>
<td>257</td>
<td>201</td>
<td>32</td>
<td>256</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>32</td>
<td>666</td>
<td>63.1</td>
<td>663</td>
<td>63.4</td>
<td>664</td>
<td>63.3</td>
<td>32</td>
<td>635</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>32</td>
<td>228</td>
<td>148</td>
<td>227</td>
<td>149</td>
<td>228</td>
<td>148</td>
<td>32</td>
<td>208</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>32</td>
<td>214</td>
<td>262</td>
<td>214</td>
<td>262</td>
<td>214</td>
<td>262</td>
<td>32</td>
<td>214</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>32</td>
<td>356</td>
<td>103</td>
<td>356</td>
<td>103</td>
<td>357</td>
<td>103</td>
<td>32</td>
<td>356</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>32</td>
<td>547</td>
<td>97.0</td>
<td>548</td>
<td>96.8</td>
<td>547</td>
<td>96.9</td>
<td>32</td>
<td>546</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>32</td>
<td>290</td>
<td>289</td>
<td>300</td>
<td>279</td>
<td>290</td>
<td>289</td>
<td>32</td>
<td>290</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>32</td>
<td>480</td>
<td>72.1</td>
<td>480</td>
<td>72.1</td>
<td>479</td>
<td>72.1</td>
<td>32</td>
<td>478</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The AMD64 AOCC Compiler Suite is available at http://developer.amd.com/amd-aocc/

Submit Notes

The config file option 'submit' was used.
'numactl' was used to bind copies to the cores.
See the configuration file for details.

Operating System Notes

'uulimit -s unlimited' was used to set environment stack size limit
'uulimit -l 2097152' was used to set environment locked pages in memory limit
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

To limit dirty cache to 8% of memory, 'sysctl -w vm.dirty_ratio=8' run as root.
To limit swap usage to minimum necessary, 'sysctl -w vm.swappiness=1' run as root.
To free node-local memory and avoid remote memory usage,
'sysctl -w vm.zone_reclaim_mode=1' run as root.
To clear filesystem caches, 'sync; sysctl -w vm.drop_caches=3' run as root.
To disable address space layout randomization (ASLR) to reduce run-to-run variability, 'sysctl -w kernel.randomize_va_space=0' run as root.

(Continued on next page)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)

Operating System Notes (Continued)
To enable Transparent Hugepages (THP) only on request for base runs, 'echo madvise > /sys/kernel/mm/transparent_hugepage/enabled' run as root.
To enable THP for all allocations for peak runs, 'echo always > /sys/kernel/mm/transparent_hugepage/enabled' and 'echo always > /sys/kernel/mm/transparent_hugepage/defrag' run as root.

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
    ":/home/cpu2017/amd_rate_aocc300_milan_B_lib/lib;/home/cpu2017/amd_rate_aocc300_milan_B_lib/lib32:" 
MALLOC_CONF = "retain:true"
Environment variables set by runcpu during the 523.xalancbmk_r peak run:
MALLOC_CONF = "thp:never"

General Notes
Binaries were compiled on a system with 2x AMD EPYC 7742 CPU + 1TiB Memory using OpenSUSE 15.2
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc: configured and built with GCC v4.8.2 in RHEL 7.4 (No options specified) 
jemalloc 5.1.0 is available here:
https://github.com/jemalloc/jemalloc/releases/download/5.1.0/jemalloc-5.1.0.tar.bz2

Platform Notes
BIOS Configuration
SMT Mode set to Auto
NUMA nodes per socket set to NPS4
ACPI SRAT L3 Cache As NUMA Domain set to Enabled
DRAM Scrub Time set to Disabled
Determinism Slider set to Power
Memory Interleaving set to Auto
APBDIS set to 1

(Continued on next page)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)

<table>
<thead>
<tr>
<th>SPEC CPU®2017 Integer Rate Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_base = 126</td>
</tr>
<tr>
<td>SPECrate®2017_int_peak = 130</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2021
Hardware Availability: Jun-2021
Tested by: Cisco Systems
Software Availability: Jun-2021

Platform Notes (Continued)
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on localhost Thu Nov 18 05:51:36 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: AMD EPYC 7252 8-Core Processor
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 8
  siblings: 16
  physical 0: cores 0 1 4 5 8 9 12 13
  physical 1: cores 0 1 4 5 8 9 12 13

From lscpu from util-linux 2.36.2:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 43 bits physical, 48 bits virtual
CPU(s): 32
On-line CPU(s) list: 0–31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 8
Vendor ID: AuthenticAMD
CPU family: 23
Model: 49
Model name: AMD EPYC 7252 8-Core Processor
Stepping: 0
Frequency boost: enabled
CPU MHz: 2154.699
CPU max MHz: 3100.0000
CPU min MHz: 1500.0000
BogoMIPS: 6188.23
Virtualization: AMD-V
L1d cache: 512 KiB
L1i cache: 512 KiB
L2 cache: 8 MiB
L3 cache: 128 MiB
NUMA node0 CPU(s): 0, 1, 16, 17
NUMA node1 CPU(s): 2, 3, 18, 19

(Continued on next page)
## Platform Notes (Continued)

| NUMA node2 CPU(s): | 4,5,20,21 |
| NUMA node3 CPU(s): | 6,7,22,23 |
| NUMA node4 CPU(s): | 8,9,24,25 |
| NUMA node5 CPU(s): | 10,11,26,27 |
| NUMA node6 CPU(s): | 12,13,28,29 |
| NUMA node7 CPU(s): | 14,15,30,31 |

Vulnerability Itlb multihit: Not affected
Vulnerability L1tf: Not affected
Vulnerability Mds: Not affected
Vulnerability Meltdown: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitization
Vulnerability Spectre v2: Mitigation; Full AMD retpoline, IBPB conditional, IBRS_FW, STIBP conditional, RSB filling
Vulnerability Srbd:s: Not affected
Vulnerability Tsx async abort: Not affected
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush mmx fxsr sse sse2 ht syscall nx mmxext fxsr_opt pdpe1gb rdtsscp lm constant_tsc rep_good nopl nonstop_tsc cpuid extd_apicid aperfmperf pni pclmulqdq monitor ssse3 fma cx16 sse4_1 sse4_2 movbe popcnt aes xsave avx f16c rdrand lahf_lm cmp_legacy svm extapic cr8_legacy abm sse4a misalignsse 3dnowprefetch osvw ibs skinit wdt tce topoext perfctr_core perfctr_nb bpext perfctr_llc mwaltx cpb cat_l3 cdp_l3 hw_pstate sme ssbd mba sev ibrs ibpb stibp vmmcall sev_es fsgsbase bm1l avx2 smep bm12 cqm rdtd_r dseed adx clflushopt clwb sha_ni xsaveopt xsavec xsave savel savelc cqm_occumpull cqm_mbb_total cqm_mbb_local clzero irperf xsaverepr wmbnoinvd arat npt lbrv svm_lock nrip_save tsc_scale vmsvc_clean flushbyasid decodeassists pausefilter pfthreshold avic v_vmsave_vmload vgif umip rdpid overflow_recov succor smca

From lscpu --cache:
```
NAME ONE-SIZE ALL-SIZE WAYS TYPE LEVEL SETS PHY-LINE COHERENCY-SIZE
L1d 32K 512K 8 Data 1 64 1 64
L1i 32K 512K 8 Instruction 1 64 1 64
L2 512K 8M 8 Unified 2 1024 1 64
L3 16M 128M 16 Unified 3 16384 1 64
```

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 8 nodes (0-7)
node 0 cpus: 0 1 16 17
node 0 size: 257863 MB
node 0 free: 257890 MB

---

(Continued on next page)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)

| SPECrate®2017_int_base = 126 |
| SPECrate®2017_int_peak = 130 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2021
Hardware Availability: Jun-2021
Tested by: Cisco Systems
Software Availability: Jun-2021

**Platform Notes (Continued)**

node 1 cpus: 2 3 18 19
node 1 size: 258046 MB
node 1 free: 257873 MB
node 2 cpus: 4 5 20 21
node 2 size: 258046 MB
node 2 free: 257805 MB
node 3 cpus: 6 7 22 23
node 3 size: 245937 MB
node 3 free: 245791 MB
node 4 cpus: 8 9 24 25
node 4 size: 258046 MB
node 4 free: 257841 MB
node 5 cpus: 10 11 26 27
node 5 size: 258046 MB
node 5 free: 257911 MB
node 6 cpus: 12 13 28 29
node 6 size: 258046 MB
node 6 free: 257845 MB
node 7 cpus: 14 15 30 31
node 7 size: 258045 MB
node 7 free: 257845 MB
node distances:

```
+----------------+----------------+----------------+----------------+----------------+----------------+----------------+----------------+
|      0      |       1       |       2       |       3       |       4       |       5       |       6       |       7       |
+----------------+----------------+----------------+----------------+----------------+----------------+----------------+----------------+
+----------------+----------------+----------------+----------------+----------------+----------------+----------------+----------------+
```

From /proc/meminfo
MemTotal: 2101293916 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has ondemand

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP3"
VERSION_ID="15.3"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
ID="sles"
## SPEC CPU 2017 Integer Rate Result

###  SPEC CPU 2017 Integer Rate Result

**Cisco Systems**

**Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)**

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Nov-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Jun-2021</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Jun-2021</td>
</tr>
</tbody>
</table>

**SPECratë 2017_int_base** = 126

**SPECratë 2017_int_peak** = 130

---

### Platform Notes (Continued)

- ID LIKE="suse"
- ANSI_COLOR="0;32"
- CPE_NAME="cpe:/o:suse:sles:15:sp3"

```bash
uname -a:
   Linux localhost 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9) x86_64
   x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- **CVE-2018-12207 (iTLB Multihit):** Not affected
- **CVE-2018-3620 (L1 Terminal Fault):** Not affected
- **Microarchitectural Data Sampling:** Not affected
- **CVE-2017-5754 (Meltdown):** Not affected
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Full AMD retpoline, IBPB: conditional, IBRS_FW, STIBP: conditional, RSB filling
- **CVE-2020-0543 (Special Register Buffer Data Sampling):** Not affected
- **CVE-2019-11135 (TSX Asynchronous Abort):** Not affected

run-level 3 Nov 18 05:34

SPEC is set to: /home/cpu2017

```bash
From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C225-M6S
Serial: WZP252309U3
```

Additional information from dmidecode 3.2 follows. **WARNING:** Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

- 16x 0xCE00 M386AAG40AM3-CWE 128 GB 4 rank 3200

BIOS:

- BIOS Vendor: Cisco Systems Inc
- BIOS Version: C225M6.4.2.1c.0.0806211349

(Continued on next page)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2021
Tested by: Cisco Systems
Software Availability: Jun-2021

Platform Notes (Continued)

BIOS Date: 08/06/2021
BIOS Revision: 5.14

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
------------------------------------------------------------------------------

================================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
================================================================================

================================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
------------------------------------------------------------------------------

================================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
(Continued on next page)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)

SPECRate\textsuperscript{®}2017\_int\_base = 126
SPECRate\textsuperscript{®}2017\_int\_peak = 130

---

**Compiler Version Notes (Continued)**

**InstalledDir:** /opt/AMD/aocc-compiler-3.0.0/bin

---

C++ | 523.xalancbmk\_r(peak)

AMD clang version 12.0.0 (CLANG: AOCC\_3.0.0-Build\#78 2020\_12\_10) (based on LLVM Mirror.Version.12.0.0)
Target: i386\_unknown\_linux\_gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

---

C++ | 520.omnetpp\_r(base, peak) 523.xalancbmk\_r(base)

531.deepsjeng\_r(base, peak) 541.leela\_r(base, peak)

AMD clang version 12.0.0 (CLANG: AOCC\_3.0.0-Build\#78 2020\_12\_10) (based on LLVM Mirror.Version.12.0.0)
Target: x86\_64\_unknown\_linux\_gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

---

C++ | 523.xalancbmk\_r(peak)

AMD clang version 12.0.0 (CLANG: AOCC\_3.0.0-Build\#78 2020\_12\_10) (based on LLVM Mirror.Version.12.0.0)
Target: i386\_unknown\_linux\_gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

---

C++ | 520.omnetpp\_r(base, peak) 523.xalancbmk\_r(base)

531.deepsjeng\_r(base, peak) 541.leela\_r(base, peak)

AMD clang version 12.0.0 (CLANG: AOCC\_3.0.0-Build\#78 2020\_12\_10) (based on LLVM Mirror.Version.12.0.0)
Target: x86\_64\_unknown\_linux\_gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

---

Fortran | 548.exchange2\_r(base, peak)

(Continued on next page)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)

SPECrater®2017_int_base = 126
SPECrater®2017_int_peak = 130

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2021

Tested by: Cisco Systems
Hardware Availability: Jun-2021
Software Availability: Jun-2021

Compiler Version Notes (Continued)

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

Base Compiler Invocation

C benchmarks:
clang

C++ benchmarks:
clang++

Fortran benchmarks:
flang

Base Portability Flags

500.perlbench_r: -DSPEC_LINUX_X64 -DSPEC_LP64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -Wl,-allow-multiple-definition -Wl, -mllvm -Wl,-enable-licm-vrp
-flto -Wl,-mllvm -Wl,-region-vectorize
-Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -O3 -ffast-math
-march=znver3 -fveclib=AMDLIBM -fstruct-layout=5

(Continued on next page)
Cisco Systems

Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Base Optimization Flags (Continued)

C benchmarks (continued):
-mlirv -unroll-threshold=50 -mlirv -inline-threshold=1000
-fremap-arrays -mlirv -function-specialize -flv-function-specialization
-mlirv -enable-gvn-hoist -mlirv -global-vectorize-slp=true
-mlirv -enable-licm-vrp -mlirv -reduce-array-computations=3 -z muldefs
-lamdlibm -ljemalloc -lflang -lflangrti

C++ benchmarks:
-m64 -std=c++98 -Wl,-mlirv -Wl,-do-block-reorder=aggressive -flto
-Wl,-mlirv -Wl,-region-vectorize -Wl,-mlirv -Wl,-function-specialize
-Wl,-mlirv -Wl,-align-all-nofallthru-blocks=6
-Wl,-mlirv -Wl,-reduce-array-computations=3 -O3 -ffast-math
-march=znver3 -fveclib=AMDLIBM -mlirv -enable-partial-unswitch
-mlirv -unroll-threshold=100 -finline-aggressive
-flv-function-specialization -mlirv -loop-unswitch-threshold=200000
-mlirv -reordered-loops -mlirv -aggressive-loop-unswitch
-mlirv -extra-vectorizer-passes -mlirv -reduce-array-computations=3
-mlirv -global-vectorize-slp=true -mlirv -convert-pow-exp-to-int=false
-g muldefs -mlirv -do-block-reorder=aggressive
-flv-function-elimination -fvisibility=hidden -lamdlibm
-ljemalloc -lflang -lflangrti

Fortran benchmarks:
-m64 -Wl,-mlirv -Wl,-inline-recursion=4
-Wl,-mlirv -Wl,-lsr-in-nested-loop -Wl,-mlirv -Wl,-enable-iv-split
-flto -Wl,-mlirv -Wl,-region-vectorize
-Wl,-mlirv -Wl,-function-specialize
-Wl,-mlirv -Wl,-align-all-nofallthru-blocks=6
-Wl,-mlirv -Wl,-reduce-array-computations=3 -O3 -ffast-math
-march=znver3 -fveclib=AMDLIBM -z muldefs -mlirv -unroll-aggressive
-mlirv -unroll-threshold=500 -lamdlibm -ljemalloc -lflang -lflangrti

Base Other Flags

C benchmarks:
-Who-unused-command-line-argument

C++ benchmarks:
-Who-unused-command-line-argument
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrates: 2017_int_base = 126
SPECrates: 2017_int_peak = 130

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2021
Hardware Availability: Jun-2021
Software Availability: Jun-2021

Peak Compiler Invocation

C benchmarks:
clang

C++ benchmarks:
clang++

Fortran benchmarks:
flang

Peak Portability Flags

500.perlbench_r: -DSPEC_LINUX_X64 -DSPEC_LP64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -m64 -Wl,-allow-multiple-definition
-W1,-mllvm -Wl,-enable-licm-vrp -flto
-W1,-mllvm -Wl,-function-specialize
-W1,-mllvm -Wl,-align-all-nofallthru-blocks=6
-W1,-mllvm -Wl,-reduce-array-computations=3
-fprofile-instr-generate(pass 1)
-fprofile-instr-use(pass 2) -Ofast -march=znver3
-fveclib=AMDLIBM -fstruct-layout=7
-mllvm -unroll-threshold=50 -fremap-arrays
-flv-function-specialization -mllvm -inline-threshold=1000
-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=false
-mllvm -function-specialize -mllvm -enable-licm-vrp
-mllvm -reduce-array-computations=3 -lamdlibm -ljemalloc

502.gcc_r: -m32 -Wl,-allow-multiple-definition
-W1,-mllvm -Wl,-enable-licm-vrp -flto
## Peak Optimization Flags (Continued)

502.gcc_r (continued):
- `-Wl,-mllvm -Wl,-function-specialize -Ofast -march=znver3`  
  `-fveclib=AMDLIBM -fstruct-layout=7`  
  `-mlirm -unroll-threshold=50 -fremap-arrays`  
  `-flv-function-specialization -mllvm -inline-threshold=1000`  
  `-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true`  
  `-mllvm -function-specialize -mllvm -enable-licm-vrp`  
  `-mllvm -reduce-array-computations=3 -fgnu89-inline`  
  `-ljemalloc`

505.mcf_r: `basepeak = yes`

525.x264_r: `basepeak = yes`

557.xz_r: `-m64 -Wl,-allow-multiple-definition`
- `-Wl,-mllvm -Wl,-function-specialize`  
  `-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6`  
  `-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast`  
  `-march=znver3 -fveclib=AMDLIBM -fstruct-layout=7`  
  `-mlirm -unroll-threshold=50 -fremap-arrays`  
  `-flv-function-specialization -mllvm -inline-threshold=1000`  
  `-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true`  
  `-mllvm -function-specialize -mllvm -enable-licm-vrp`  
  `-mllvm -reduce-array-computations=3 -lamdlibm -ljemalloc`

### C++ benchmarks:

520.omnetpp_r: `-m64 -std=c++98`
- `-Wl,-mllvm -Wl,-do-block-reorder-aggressive -flto`  
  `-Wl,-mllvm -Wl,-function-specialize`  
  `-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6`  
  `-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast`  
  `-march=znver3 -fveclib=AMDLIBM -finline-aggressive`  
  `-mlirm -unroll-threshold=100 -flv-function-specialization`  
  `-mlirm -enable-licm-vrp -mlirm -reroll-loops`  
  `-mlirm -aggressive-loop-unswitch`  
  `-mlirm -reduce-array-computations=3`  
  `-mlirm -global-vectorize-slp=true`  
  `-mlirm -do-block-reorder-aggressive`  
  `-fvirtual-function-elimination -fvisibility=hidden`  
  `-lamdlibm -ljemalloc`

523.xalancbmk_r: `-m32 -Wl,-mllvm -Wl,-do-block-reorder-aggressive -flto`  
- `-Wl,-mllvm -Wl,-function-specialize`  
  `-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6`
## SPEC CPU®2017 Integer Rate Result

### Cisco Systems

Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)

| SPECrate®2017_int_base | 126 |
| SPECrate®2017_int_peak | 130 |

**CPU2017 License:** 9019  
**Test Date:** Nov-2021  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Hardware Availability:** Jun-2021  
**Software Availability:** Jun-2021

### Peak Optimization Flags (Continued)

523.xalancbmk_r (continued):
- `-Wl,-mlllvm -Wl,-reduce-array-computations=3 -Ofast`  
- `-march=znver3 -fveclib=AMDLIBM -finline-aggressive`  
- `-mlllvm -unroll-threshold=100 -flv-function-specialization`  
- `-mlllvm -enable-licm-vrp -mlllvm -reroll-loops`  
- `-mlllvm -aggressive-loop-unswitch`  
- `-mlllvm -reduce-array-computations=3`  
- `-mlllvm -global-vectorize-slp=true`  
- `-mlllvm -do-block-reorder=aggressive`  
- `-fvirtual-function-elimination -fvisibility=hidden`  
- `-ljemalloc`

531.deepsjeng_r: basepeak = yes

541.leela_r: Same as 520.omnetpp_r

### Peak Other Flags

- C benchmarks (except as noted below):
  - `-Wno-unused-command-line-argument`

502.gcc_r: `-L/usr/lib -Wno-unused-command-line-argument`  
- `-L/sppo/bin/cpu2017v115aocc3/amd_rate_aocc300_milan_A_lib/32`

- C++ benchmarks (except as noted below):
  - `-Wno-unused-command-line-argument`

523.xalancbmk_r: `-L/usr/lib -Wno-unused-command-line-argument`  
- `-L/sppo/bin/cpu2017v115aocc3/amd_rate_aocc300_milan_A_lib/32`

---

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:

# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

### Cisco UCS C225 M6 (AMD EPYC 7252 8-Core)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

### SPECrate®2017_int_base

- **SPECrate®2017_int_base = 126**

### SPECrate®2017_int_peak

- **SPECrate®2017_int_peak = 130**

---

**Test Date:** Nov-2021  
**Hardware Availability:** Jun-2021  
**Software Availability:** Jun-2021  

---

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-11-18 08:51:36-0500.  
Report generated on 2021-12-22 12:33:50 by CPU2017 PDF formatter v6442.  
Originally published on 2021-12-21.