SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

Cisco Systems

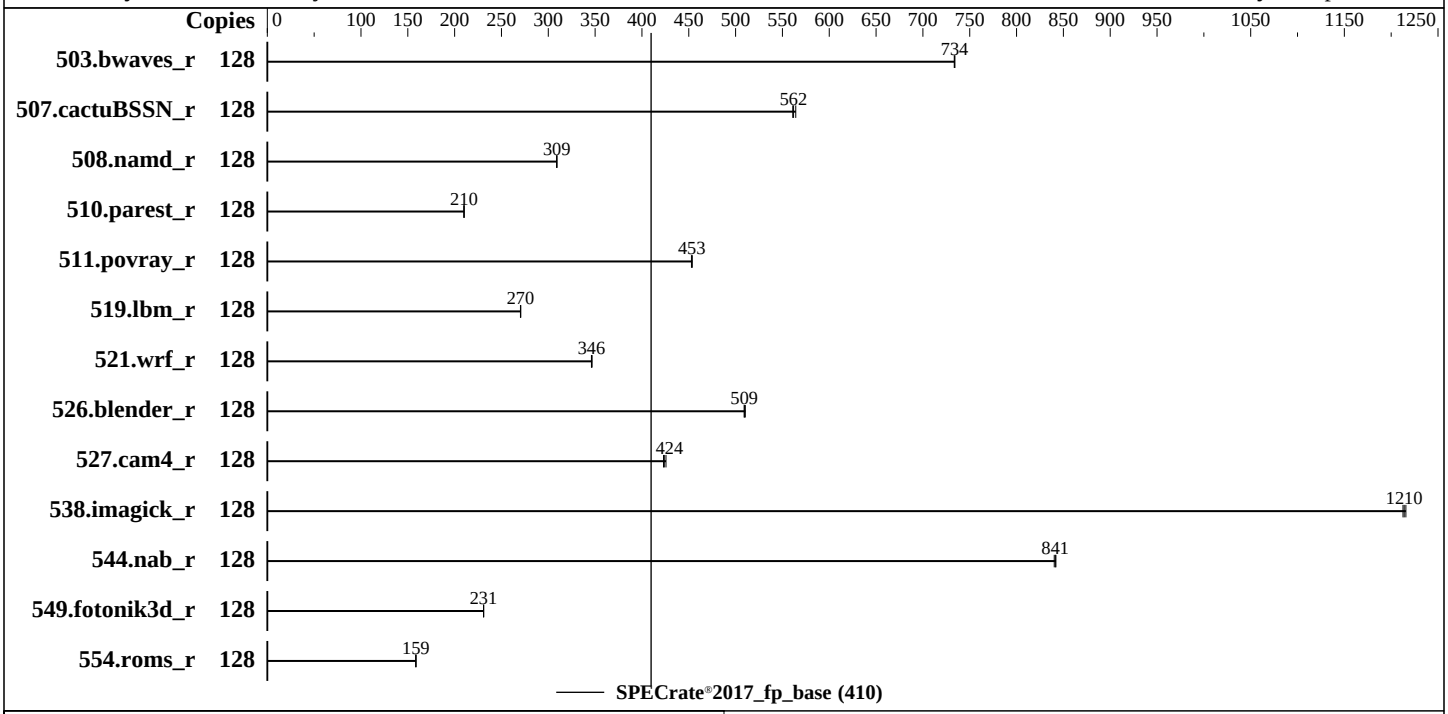
Cisco UCS X210c M6 (Intel Xeon Gold 6338, 2.00GHz)

SPECrate®2017_fp_base = 410

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021



Hardware

CPU Name:	Intel Xeon Gold 6338
Max MHz:	3200
Nominal:	2000
Enabled:	64 cores, 2 chips, 2 threads/core
Orderable:	1,2 Chips
Cache L1:	32 KB I + 48 KB D on chip per core
L2:	1.25 MB I+D on chip per core
L3:	48 MB I+D on chip per chip
Other:	None
Memory:	2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
Storage:	1 x 240 GB M.2 SSD SATA
Other:	None

Software

OS:	SUSE Linux Enterprise Server 15 SP3 5.3.18-57-default
Compiler:	C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++ Compiler Build 20210924 for Linux; Fortran: Version 2021.4.0 of Intel Fortran Compiler Classic Build 20210910 for Linux;
Parallel:	No
Firmware:	Version 5.0.1d released Aug-2021
File System:	xfs
System State:	Run level 3 (multi-user)
Base Pointers:	64-bit
Peak Pointers:	Not Applicable
Other:	jemalloc memory allocator V5.0.1
Power Management:	OS set to prefer performance at the cost of additional power usage

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Gold 6338, 2.00GHz)

SPECrate®2017_fp_base = 410

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	128	1750	733	1749	734	**1749**	**734**							
507.cactuBSSN_r	128	**288**	**562**	287	564	289	561							
508.namd_r	128	394	309	**393**	**309**	393	309							
510.parest_r	128	1596	210	1593	210	**1594**	**210**							
511.povray_r	128	660	453	**659**	**453**	659	454							
519.lbm_r	128	499	270	499	271	**499**	**270**							
521.wrf_r	128	**828**	**346**	827	347	828	346							
526.blender_r	128	383	509	382	510	**383**	**509**							
527.cam4_r	128	526	426	529	423	**528**	**424**							
538.imagick_r	128	**262**	**1210**	262	1220	263	1210							
544.nab_r	128	**256**	**841**	256	842	256	840							
549.fotonik3d_r	128	2161	231	**2160**	**231**	2159	231							
554.roms_r	128	1281	159	**1282**	**159**	1284	158							

SPECrate®2017_fp_base = 410

SPECrate®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

```
The numactl mechanism was used to bind copies to processors. The config file option 'submit'
was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.
```

Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
```

Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
```

General Notes

```
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
```

(Continued on next page)

General Notes (Continued)

```
 sync; echo 3>       /proc/sys/vm/drop_caches
 runcpu command invoked through numactl i.e.:
 numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases
```

Platform Notes

```
BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
 running on perf-blade1 Sun Nov 21 23:49:43 2021

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6338 CPU @ 2.00GHz
       2  "physical id"s (chips)
       128 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 32
       siblings  : 64
       physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
       25 26 27 28 29 30 31
       physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
       25 26 27 28 29 30 31
```

(Continued on next page)

Platform Notes (Continued)

```
From lscpu from util-linux 2.36.2:
     Architecture:                    x86_64
     CPU op-mode(s):                  32-bit, 64-bit
     Byte Order:                      Little Endian
     Address sizes:                   46 bits physical, 57 bits virtual
     CPU(s):                          128
     On-line CPU(s) list:             0-127
     Thread(s) per core:              2
     Core(s) per socket:              32
     Socket(s):                       2
     NUMA node(s):                    4
     Vendor ID:                       GenuineIntel
     CPU family:                      6
     Model:                           106
     Model name:                      Intel(R) Xeon(R) Gold 6338 CPU @ 2.00GHz
     Stepping:                        6
     CPU MHz:                         800.213
     CPU max MHz:                     3200.0000
     CPU min MHz:                     800.0000
     BogoMIPS:                        4000.00
     Virtualization:                  VT-x
     L1d cache:                       3 MiB
     L1i cache:                       2 MiB
     L2 cache:                        80 MiB
     L3 cache:                        96 MiB
     NUMA node0 CPU(s):               0-15,64-79
     NUMA node1 CPU(s):               16-31,80-95
     NUMA node2 CPU(s):               32-47,96-111
     NUMA node3 CPU(s):               48-63,112-127
     Vulnerability Itlb multihit:     Not affected
     Vulnerability L1tf:              Not affected
     Vulnerability Mds:               Not affected
     Vulnerability Meltdown:          Not affected
     Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via
     prctl and seccomp
     Vulnerability Spectre v1:        Mitigation; usercopy/swapgs barriers and __user
     pointer sanitization
     Vulnerability Spectre v2:        Mitigation; Enhanced IBRS, IBPB conditional, RSB
     filling
     Vulnerability Srbds:             Not affected
     Vulnerability Tsx async abort:   Not affected
     Flags:                           fpu vme de pse tsc msr pae mce cx8 apic sep mtrr
     pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx
     pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology
     nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2
     ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
     tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
```

(Continued on next page)

Platform Notes (Continued)

```
      epb cat_l3 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
      flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms
      invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb
      intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc
      cqm_occup_llc cqm_mbm_total cqm_mbm_local split_lock_detect wbnoinvd dtherm ida arat
      pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vbmi umip pku ospke
      avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq
      la57 rdpid fsrm md_clear pconfig flush_l1d arch_capabilities

From lscpu --cache:
     NAME ONE-SIZE ALL-SIZE WAYS TYPE        LEVEL  SETS PHY-LINE COHERENCY-SIZE
     L1d       48K       3M   12 Data            1    64        1             64
     L1i       32K       2M    8 Instruction     1    64        1             64
     L2       1.3M      80M   20 Unified         2  1024        1             64
     L3        48M      96M   12 Unified         3 65536        1             64

/proc/cpuinfo cache data
   cache size : 49152 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 64 65 66 67 68 69 70 71 72 73 74 75
  76 77 78 79
  node 0 size: 515682 MB
  node 0 free: 515263 MB
  node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 80 81 82 83 84 85 86 87 88
  89 90 91 92 93 94 95
  node 1 size: 516088 MB
  node 1 free: 515644 MB
  node 2 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 96 97 98 99 100 101 102
  103 104 105 106 107 108 109 110 111
  node 2 size: 516054 MB
  node 2 free: 515696 MB
  node 3 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 112 113 114 115 116 117
  118 119 120 121 122 123 124 125 126 127
  node 3 size: 516084 MB
  node 3 free: 515729 MB
  node distances:
  node   0   1   2   3
    0:  10  11  20  20
    1:  11  10  20  20
    2:  20  20  10  11
    3:  20  20  11  10

From /proc/meminfo
   MemTotal:       2113442860 kB
```

(Continued on next page)

Platform Notes (Continued)

```
   HugePages_Total:       0
   Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
   performance

From /etc/*release* /etc/*version*
   os-release:
      NAME="SLES"
      VERSION="15-SP3"
      VERSION_ID="15.3"
      PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
      ID="sles"
      ID_LIKE="suse"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:15:sp3"

uname -a:
   Linux perf-blade1 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9)
   x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):                          Not affected
CVE-2018-3620 (L1 Terminal Fault):                       Not affected
Microarchitectural Data Sampling:                        Not affected
CVE-2017-5754 (Meltdown):                                Not affected
CVE-2018-3639 (Speculative Store Bypass):                Mitigation: Speculative Store
                                                         Bypass disabled via prctl and
                                                         seccomp
CVE-2017-5753 (Spectre variant 1):                       Mitigation: usercopy/swapgs
                                                         barriers and __user pointer
                                                         sanitization
CVE-2017-5715 (Spectre variant 2):                      Mitigation: Enhanced IBRS, IBPB:
                                                         conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):                 Not affected

run-level 3 Nov 21 23:28

SPEC is set to: /home/cpu2017
   Filesystem     Type  Size  Used Avail Use% Mounted on
   /dev/sda3      xfs   181G   44G  137G  25% /home

From /sys/devices/virtual/dmi/id
    Vendor:         Cisco Systems Inc
    Product:        UCSX-210C-M6
```

(Continued on next page)

Platform Notes (Continued)

```
     Serial:         FCH25057AMV

  Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
  interpret this section. The 'dmidecode' program reads system data which is "intended to
  allow hardware to be accurately determined", but the intent may not be met, as there are
  frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    Memory:
      32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

  BIOS:
     BIOS Vendor:       Cisco Systems, Inc.
     BIOS Version:      X210M6.5.0.1d.0.0816211754
     BIOS Date:         08/16/2021
     BIOS Revision:     5.22

  (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++             | 508.namd_r(base) 510.parest_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
```

(Continued on next page)

Compiler Version Notes (Continued)

```
==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran         | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation.  All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

(Continued on next page)

Base Compiler Invocation (Continued)

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

(Continued on next page)

Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -ljemalloc -L/home/cpu2017/je5.0.1-64

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -ljemalloc -L/home/cpu2017/je5.0.1-64

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.2021-12-22.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revl.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.2021-12-22.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revl.xml

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-11-22 02:49:42-0500.
Report generated on 2022-02-04 12:38:32 by CPU2017 PS formatter v6442.
Originally published on 2022-02-04.