# SPEC CPU®2017 Integer Speed Result

## Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 5318Y, 2.10GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>11.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_int_peak</td>
<td>11.6</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2021</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Sep-2021</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Sep-2021</td>
</tr>
</tbody>
</table>

### Hardware
- **CPU Name:** Intel Xeon Gold 5318Y
- **Max MHz:** 3400
- **Nominal:** 2100
- **Enabled:** 48 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **Cache L2:** 1.25 MB I+D on chip per core
- **Cache L3:** 36 MB I+D on chip per chip
- **Other:** None
- **Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2933)
- **Storage:** 1 x 240 GB M.2 SSD SATA
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
- **Compiler:** C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++ Compiler Build 20210924 for Linux;
  Fortran: Version 2021.4.0 of Intel Fortran Compiler
  Classic Build 20210910 for Linux;
  C/C++: Version 2021.4.0 of Intel C/C++ Compiler
  Classic Build 20210910 for Linux;
- **Parallel:** Yes
- **Firmware:** Version 5.0.1d released Aug-2021
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage

<table>
<thead>
<tr>
<th>Threads</th>
<th>0</th>
<th>1.00</th>
<th>2.00</th>
<th>3.00</th>
<th>4.00</th>
<th>5.00</th>
<th>6.00</th>
<th>7.00</th>
<th>8.00</th>
<th>9.00</th>
<th>10.0</th>
<th>11.0</th>
<th>12.0</th>
<th>13.0</th>
<th>14.0</th>
<th>15.0</th>
<th>16.0</th>
<th>17.0</th>
<th>18.0</th>
<th>19.0</th>
<th>20.0</th>
<th>21.0</th>
<th>22.0</th>
<th>23.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>48</td>
<td></td>
<td></td>
<td></td>
<td>6.87</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>602.gcc_s</td>
<td>48</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8.04</td>
<td></td>
<td>10.6</td>
<td>10.6</td>
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<td>605.mcf_s</td>
<td>48</td>
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<td></td>
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<tr>
<td>620.omnetpp_s</td>
<td>48</td>
<td></td>
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<td>623.xalancbmk_s</td>
<td>48</td>
<td></td>
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<td>12.9</td>
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<tr>
<td>625.x264_s</td>
<td>48</td>
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<td>631.deepsjeng_s</td>
<td>48</td>
<td></td>
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<td>17.0</td>
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<td></td>
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<tr>
<td>641.leela_s</td>
<td>48</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>48</td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<td>18.8</td>
<td></td>
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<td></td>
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<td></td>
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<tr>
<td>657.xz_s</td>
<td>48</td>
<td></td>
<td></td>
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<td>22.6</td>
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<td></td>
</tr>
</tbody>
</table>

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## SPEC CPU®2017 Integer Speed Result

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Cisco UCS X210c M6 (Intel Xeon Gold 5318Y, 2.10GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>48</td>
<td>259</td>
<td>6.85</td>
<td>258</td>
<td>6.87</td>
<td>257</td>
<td>6.90</td>
<td>48</td>
<td>221</td>
<td>8.02</td>
<td>219</td>
<td>8.09</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>48</td>
<td>375</td>
<td>10.6</td>
<td>377</td>
<td>10.6</td>
<td>374</td>
<td>10.6</td>
<td>48</td>
<td>375</td>
<td>10.6</td>
<td>375</td>
<td>10.6</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>48</td>
<td>251</td>
<td>18.8</td>
<td>251</td>
<td>18.8</td>
<td>249</td>
<td>19.0</td>
<td>48</td>
<td>251</td>
<td>18.8</td>
<td>251</td>
<td>18.8</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>48</td>
<td>144</td>
<td>11.3</td>
<td>139</td>
<td>11.7</td>
<td>143</td>
<td>11.4</td>
<td>48</td>
<td>144</td>
<td>11.3</td>
<td>139</td>
<td>11.7</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>48</td>
<td>110</td>
<td>12.9</td>
<td>110</td>
<td>12.9</td>
<td>109</td>
<td>13.0</td>
<td>48</td>
<td>110</td>
<td>12.9</td>
<td>110</td>
<td>12.9</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>48</td>
<td>106</td>
<td>16.7</td>
<td>106</td>
<td>16.7</td>
<td>106</td>
<td>16.7</td>
<td>48</td>
<td>104</td>
<td>17.0</td>
<td>104</td>
<td>17.0</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>48</td>
<td>249</td>
<td>5.76</td>
<td>249</td>
<td>5.76</td>
<td>249</td>
<td>5.76</td>
<td>48</td>
<td>249</td>
<td>5.76</td>
<td>249</td>
<td>5.76</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>48</td>
<td>157</td>
<td>18.8</td>
<td>158</td>
<td>18.7</td>
<td>156</td>
<td>18.8</td>
<td>48</td>
<td>157</td>
<td>18.8</td>
<td>158</td>
<td>18.7</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>48</td>
<td>274</td>
<td>22.6</td>
<td>272</td>
<td>22.7</td>
<td>274</td>
<td>22.6</td>
<td>48</td>
<td>274</td>
<td>22.6</td>
<td>272</td>
<td>22.7</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,scatter"
- MALLOC_CONF = "retain:true"
- OMP_STACKSIZE = "192M"

### General Notes

Binary compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

csync; echo 3 > /proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
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SPEC CPU®2017 Integer Speed Result

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General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Intel Hyper-Threading Technology set to Disable
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on perf-blade2 Fri Dec 10 01:20:25 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5318Y CPU @ 2.10GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 48
On-line CPU(s) list: 0-47

(Continued on next page)
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Platform Notes (Continued)

node distances:
node  0  1
0:  10  20
1:  20  10

From /proc/meminfo
MemTotal:       2113462332 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"
uname -a:
Linux perf-blade2 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5753 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2017-5715 (Spectre variant 2): Not affected
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Dec 10 00:08
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SPECs 2017 Int. Speed Result

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Platform Notes (Continued)

SPEC is set to: /home/cpu2017
Filesitem     Type   Size  Used  Avail  Use%  Mounted on
/dev/sda4    btrfs  218G  43G   176G  20%  /home

From /sys/devices/virtual/dmi/id
Vendor:       Cisco Systems Inc
Product:      UCSX-210C-M6
Serial:       FCH250671KR

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory: 32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2933

BIOS: BIOS Vendor: Cisco Systems, Inc.
BIOS Version: X210M6.5.0.1d.0.0816211754
BIOS Date: 08/16/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C       | 600.perlbench_s(peak) |
|----------------------------------------------------------------------------------------------|
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64,
Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

==============================================================================
| C       | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak) |
| | 625.x264_s(base, peak) 657.xz_s(base, peak) |
|----------------------------------------------------------------------------------------------|
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

==============================================================================
| C       | 600.perlbench_s(peak) |
|----------------------------------------------------------------------------------------------|

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Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 5318Y, 2.10GHz)

SPECspeed®2017_int_base = 11.4
SPECspeed®2017_int_peak = 11.6

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort
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Cisco UCS X210c M6 (Intel Xeon Gold 5318Y, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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SPECspeed®2017_int_base = 11.4
SPECspeed®2017_int_peak = 11.6
Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-DSPEC_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/home/cpu2017/je5.0.1-64 -ljemalloc

C++ benchmarks:
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries

Peak Compiler Invocation

C benchmarks (except as noted below):
icx

600.perlbench_s: icc

C++ benchmarks:
icpx

(Continued on next page)
Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries -L/home/cpu2017/je5.0.1-64
-ljemalloc

602.gcc_s: -m64 -std=c11 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -L/home/cpu2017/je5.0.1-64
-ljemalloc

605.mcf_s: basepeak = yes

625.x264_s: -DSPEC_OPENMP -fiopenmp -std=c11 -m64 -Wl,-z,muldefs
-xCORE-AVX512 -flto -O3 -ffast-math
-qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries -L/home/cpu2017/je5.0.1-64
-ljemalloc

657.xz_s: basepeak = yes

C++ benchmarks:

620.omnetpp_s: basepeak = yes

623.xalancbmk_s: basepeak = yes

631.deepsjeng_s: basepeak = yes

(Continued on next page)
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| SPECspeed®2017_int_base = 11.4 |
| SPECspeed®2017_int_peak = 11.6 |

- **CPU2017 License:** 9019
- **Test Sponsor:** Cisco Systems
- **Tested by:** Cisco Systems
- **Test Date:** Dec-2021
- **Hardware Availability:** Sep-2021
- **Software Availability:** Sep-2021

### Peak Optimization Flags (Continued)

641.leela_s: basepeak = yes

Fortran benchmarks:

648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-12-10 04:20:25-0500.
Originally published on 2022-01-04.