## Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Platinum 8368, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 465</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = Not Run</td>
</tr>
</tbody>
</table>

### CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Dec-2021

Hardware Availability: Sep-2021

Software Availability: Sep-2021

<table>
<thead>
<tr>
<th>CPU Name: Intel Xeon Platinum 8368</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max MHz: 3400</td>
</tr>
<tr>
<td>Nominal: 2400</td>
</tr>
<tr>
<td>Enabled: 76 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable: 1,2 Chips</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 48 KB D on chip per core</td>
</tr>
<tr>
<td>L2: 1.25 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3: 57 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)</td>
</tr>
<tr>
<td>Storage: 1 x 240 GB M.2 SSD SATA</td>
</tr>
<tr>
<td>Other: None</td>
</tr>
</tbody>
</table>

### OS:

SUSE Linux Enterprise Server 15 SP3 5.3.18-57-default

### Compiler:

C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++ Compiler Build 20210924 for Linux;
Fortran: Version 2021.4.0 of Intel Fortran Classic Build 20210910 for Linux;

### Parallel:

No

### Firmware:

Version 5.0.1d released Aug-2021

### File System:

xfs

### System State:

Run level 3 (multi-user)

### Base Pointers:

64-bit

### Peak Pointers:

Not Applicable

### Power Management:

BIOS and OS set to prefer performance at the cost of additional power usage

### Hardware

#### 503.bwaves_r

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_fp_base (465)</th>
</tr>
</thead>
<tbody>
<tr>
<td>152</td>
<td>619</td>
</tr>
</tbody>
</table>

#### 507.cactuBSSN_r

<table>
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<tbody>
<tr>
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<td>419</td>
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#### 508.namd_r

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<tbody>
<tr>
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<td>213</td>
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#### 510.parest_r

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<tbody>
<tr>
<td>152</td>
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#### 511.povray_r

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<tbody>
<tr>
<td>152</td>
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#### 519.lbm_r

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#### 521.wrf_r

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<tr>
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#### 526.blender_r

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<tr>
<td>152</td>
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#### 527.cam4_r

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<tbody>
<tr>
<td>152</td>
<td>1150</td>
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#### 538.imagick_r

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#### 544.nab_r

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#### 549.fotonik3d_r

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#### 554.roms_r

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

SPECrate®2017_fp_base = 465
SPECrate®2017_fp_peak = Not Run

Results Table

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<th>Ratio</th>
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<td></td>
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SPECrate®2017_fp_base = 465
SPECrate®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
General Notes (Continued)

sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDC Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on perf-bladel Tue Dec 14 04:16:46 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Platinum 8368 CPU @ 2.40GHz
  2 "physical id"s (chips)
  152 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 38
siblings : 76
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
  25 26 27 28 29 30 31 32 33 34 35 36 37
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
  25 26 27 28 29 30 31 32 33 34 35 36 37

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Platinum 8368, 2.40GHz)  

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Dec-2021  
Hardware Availability: Sep-2021  
Software Availability: Sep-2021

**SPECrate®2017_fp_base** = 465  
**SPECrate®2017_fp_peak** = Not Run

Platform Notes (Continued)

From `lscpu` from `util-linux 2.36.2`:
- **Architecture:** x86_64  
- **CPU op-mode(s):** 32-bit, 64-bit  
- **Byte Order:** Little Endian  
- **Address sizes:** 46 bits physical, 57 bits virtual  
- **CPU(s):** 152  
- **On-line CPU(s) list:** 0-151  
- **Thread(s) per core:** 2  
- **Core(s) per socket:** 38  
- **Socket(s):** 2  
- **NUMA node(s):** 2  
- **Vendor ID:** GenuineIntel  
- **CPU family:** 6  
- **Model:** 106  
- **Model name:** Intel(R) Xeon(R) Platinum 8368 CPU @ 2.40GHz  
- **Stepping:** 6  
- **CPU MHz:** 800.000  
- **CPU max MHz:** 3400.0000  
- **CPU min MHz:** 800.0000  
- **BogoMIPS:** 4800.00  
- **Virtualization:** VT-x  
- **L1d cache:** 3.6 MiB  
- **L1i cache:** 2.4 MiB  
- **L2 cache:** 95 MiB  
- **L3 cache:** 114 MiB  
- **NUMA node0 CPU(s):** 0-37,76-113  
- **NUMA node1 CPU(s):** 38-75,114-151  
- **Vulnerability Itlb multihit:** Not affected  
- **Vulnerability L1tf:** Not affected  
- **Vulnerability Mds:** Not affected  
- **Vulnerability Meltdown:** Not affected  
- **Vulnerability Spec store bypass:** Mitigation; Speculative Store Bypass disabled via prctl and seccomp  
- **Vulnerability Spectre v1:** Mitigation; usercopy/swapgs barriers and __user pointer sanitization  
- **Vulnerability Spectre v2:** Mitigation; Enhanced IBRS, IBPB conditional, RSB filling  
- **Vulnerability Srbds:** Not affected  
- **Vulnerability Txs async abort:** Not affected  
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelpgb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1uese4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault eb pcat l3 invpcid_single ssbd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmihle avx2 smep bmi2 erms

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Platinum 8368, 2.40GHz)

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Platform Notes (Continued)

invpcid rtm cqcm rdt_a avx512f avx512dq rsseed adx smap avx512ifma clflushopt clwb
intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsavec xgetbv1 xsavees cqmllc
cqmmnlu llc cqmmnmuall cqmmnmutotal cqmmnmutlocal split_lock_detect wbnoinv dtherm ida arat
pln pts hwp_act_window hwp_epp hwp_pkg_req avx512vbm umip pku ospke
avx512_vbmi2 gfnl vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq
la57 rdpid fslr md_clear pconfig flush_1ld arch_capabilities

From lscpu --cache:
NAME ONE-SIZE ALL-SIZE WAYS TYPE LEVEL SETS PHY-LINE COHERENCY-SIZE
L1d 48K 3.6M 12 Data 1 64 1 64
L1i 32K 2.4M 8 Instruction 1 64 1 64
L2 1.3M 95M 20 Unified 2 1024 1 64
L3 57M 114M 12 Unified 3 77824 1 64

/proc/cpuinfo cache data
    cache size : 58368 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55
56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82
83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106
107 108 109 110 111 112 113
node 1 cpus: 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61
62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87
88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109
node 1 size: 1031768 MB
node 1 free: 1030323 MB
node distances:
    node 0 1
    0: 10 20
    1: 20 10

From /proc/meminfo
MemTotal: 2113438168 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
    NAME="SLES"

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Platinum 8368, 2.40GHz)  

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**Platform Notes (Continued)**

```
VERSION="15-SP3"
VERSION_ID="15.3"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp3"
```

```
uname -a:
Linux perf-blade1 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9)
x86_64 x86_64 x86_64 GNU/Linux
```

**Kernel self-reported vulnerability status:**

- CVE-2018-12207 (iTLB Multihit): Not affected
- CVE-2018-3620 (L1 Terminal Fault): Not affected
- Microarchitectural Data Sampling: Not affected
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2018-3639 (Speculative Store Bypass):
  Mitigation: Speculative Store Bypass disabled via prctl and seccomp

- CVE-2017-5753 (Spectre variant 1):
  Mitigation: usercopy/swappgs barriers and __user pointer sanitation

- CVE-2017-5715 (Spectre variant 2):
  Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

- CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
- CVE-2019-11135 (TSX Asynchronous Abort): Not affected

**run-level 3 Dec 13 20:44**

**SPEC is set to:** /home/cpu2017
```
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda3 xfs 181G 54G 128G 30% /home
```

**From /sys/devices/virtual/dmi/id**
```
Vendor: Cisco Systems Inc
Product: UCSX-210C-M6
Serial: FCH25057AMV
```

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

**Memory:**
```
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200
```
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Platinum 8368, 2.40GHz)

SPECrater®2017_fp_base = 465
SPECrater®2017_fp_peak = Not Run

Platform Notes (Continued)

BIOS:
- BIOS Vendor: Cisco Systems, Inc.
- BIOS Version: X210M6.5.0.1d.0.0816211754
- BIOS Date: 08/16/2021
- BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

C | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

C++ | 508.namd_r(base) 510.parest_r(base)

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C++, C | 511.povray_r(base) 526.blender_r(base)

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**SPEC CPU** 2017 Floating Point Rate Result

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Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

Fortran | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)

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Fortran, C | 521.wrf_r(base) 527.cam4_r(base)

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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924
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Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Platinum 8368, 2.40GHz)

SPECrater\textsuperscript{\textregistered}2017\_fp\_base = 465

SPECrater\textsuperscript{\textregistered}2017\_fp\_peak = Not Run

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**Test Date:** Dec-2021

**Hardware Availability:** Sep-2021

**Software Availability:** Sep-2021

---

### Base Portability Flags

- 503.bwaves\_r: -DSPEC\_LP64
- 507.cactuBSSN\_r: -DSPEC\_LP64
- 508.namd\_r: -DSPEC\_LP64
- 510.parest\_r: -DSPEC\_LP64
- 511.povray\_r: -DSPEC\_LP64
- 519.lbm\_r: -DSPEC\_LP64
- 521.wrf\_r: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG -convert big_endian
- 526.blender\_r: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG
- 527.cam4\_r: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG
- 538.imagick\_r: -DSPEC\_LP64
- 544.nab\_r: -DSPEC\_LP64
- 549.fotonik3d\_r: -DSPEC\_LP64
- 554.roms\_r: -DSPEC\_LP64

### Base Optimization Flags

**C benchmarks:**

```bash
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64
```

**C++ benchmarks:**

```bash
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64
```

**Fortran benchmarks:**

```bash
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64
```

**Benchmarks using both Fortran and C:**

```bash
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -ljemalloc -L/home/cpu2017/je5.0.1-64
```

**Benchmarks using both C and C++:**

```bash
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
```

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Platinum 8368, 2.40GHz)

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<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Sep-2021</td>
</tr>
</tbody>
</table>

**SPEC CPU®2017 Floating Point Rate Result**

**SPECrate®2017_fp_base = 465**

**SPECrate®2017_fp_peak = Not Run**

### Base Optimization Flags (Continued)

Benchmarks using both C and C++ (continued):
- `mbranches-within-32B-boundaries`
- `ljemalloc`
- `-L/home/cpu2017/je5.0.1-64`

Benchmarks using Fortran, C, and C++:
- `-w`
- `-m64`
- `-std=c11`
- `-Wl,-z,muldefs`
- `-xCORE-AVX512`
- `-Ofast`
- `-ffast-math`
- `-flto`
- `-mfpmath=sse`
- `-funroll-loops`
- `-z,muldefs`
- `-ljemalloc`
- `-L/home/cpu2017/je5.0.1-64`

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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