Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4310, 2.10GHz)

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**SPEC CPU®2017 Floating Point Rate Result**

**Cisco Systems**
Cisco UCS X210c M6 (Intel Xeon Silver 4310, 2.10GHz)

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**Submit Notes**
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**
Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/intel/tbb/2021.4.0/env/../lib/intel64/gcc4.8:/home/intel/mpi/2021 .4.0/libfabric/lib:/home/intel/mpi/2021.4.0//lib/release:/home/intel/mp i/2021.4.0/lib:/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64 _lin:/home/intel/compiler/2021.4.0/linux/lib:/home/intel/clck/2021.4.0/l ib/intel64:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4310, 2.10GHz)

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes
BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDC Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on perf-blade3 Sat Dec 11 16:55:05 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4310 CPU @ 2.10GHz
 2 "physical id"s (chips)
48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 24

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4310, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrater®2017_fp_base = 207
SPECrater®2017_fp_peak = Not Run

Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Platform Notes (Continued)

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11

From lscpu from util-linux 2.33.1:

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 48
On-line CPU(s) list: 0-47
Thread per core: 2
Core(s) per socket: 12
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4310 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 3214.171
CPU max MHz: 3300.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 18432K
NUMA node0 CPU(s): 0-5, 24-29
NUMA node1 CPU(s): 6-11, 30-35
NUMA node2 CPU(s): 12-17, 36-41
NUMA node3 CPU(s): 18-23, 42-47
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrunc pdcm cmid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni axv512bw avx512vl xsaveopt xsavec xsaveopt xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local wbinvd dtherm ida arat pln pts hwp act window hwp epp hwp_pkg_req avx512v bmi umip pku ospke avx512_vbmi2 gfn vaes vpcmldqd avx512_vnni avx512_bitalg tm avx512_vpoptd dq 1a57 rdpid md_clear pconfig flush_lid arch_capabilities

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**Cisco Systems**
Cisco UCS X210c M6 (Intel Xeon Silver 4310, 2.10GHz)  

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**CPU2017 License:** 9019  
**Test Date:** Dec-2021  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Sep-2021  
**Tested by:** Cisco Systems  
**Software Availability:** Sep-2021  

**Platform Notes (Continued)**

```plaintext
/proc/cpuinfo cache data  
cache size : 18432 KB

From numacl --hardware  
WARNING: a numacl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)  
node 0 cpus: 0 1 2 3 4 5 24 25 26 27 28 29  
node 0 size: 515686 MB  
node 0 free: 515351 MB  
node 1 cpus: 6 7 8 9 10 11 30 31 32 33 34 35  
node 1 size: 516058 MB  
node 1 free: 515768 MB  
node 2 cpus: 12 13 14 15 16 17 36 37 38 39 40 41  
node 2 size: 516092 MB  
node 2 free: 515870 MB  
node 3 cpus: 18 19 20 21 22 23 42 43 44 45 46 47  
node 3 size: 516089 MB  
node 3 free: 515876 MB  
node distances:  
node 0 1 2 3  
0: 10 11 20 20  
1: 11 10 20 20  
2: 20 20 10 11  
3: 20 20 11 10

From /proc/meminfo  
MemTotal: 2113461676 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*  
os-release:  
NAME="SLES"  
VERSION="15-SP2"  
VERSION_ID="15.2"  
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"  
ID="sles"  
ID_LIKE="suse"  
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:  
Linux perf-blade3 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba)  
x86_64 x86_64 x86_64 GNU/Linux

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4310, 2.10GHz)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4310, 2.10GHz)

Compiler Version Notes

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Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4310, 2.10GHz)

SPECratenet_2017_fp_base = 207
SPECratenet_2017_fp_peak = Not Run

CPU2017 License: 9019
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Compiler Version Notes (Continued)

Fortran, C | 521.wrf_r(base) 527.cam4_r(base)

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char

(Continued on next page)
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**SPECrate®2017_fp_base = 207**
**SPECrate®2017_fp_peak = Not Run**

### Base Portability Flags (Continued)

- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

### Base Optimization Flags

#### C benchmarks:
- `-w` `-std=c11` `-m64` `-Wl,-z,-m64,` `muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math`
- `-flto` `-mfpmath=sse` `-funroll-loops` `-qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries` `-ljemalloc` `-L/home/cpu2017/je5.0.1-64`

#### C++ benchmarks:
- `-w` `-m64` `-Wl,-z,-m64,` `muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math` `-flto`
- `-mfpmath=sse` `-funroll-loops` `-qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries` `-ljemalloc` `-L/home/cpu2017/je5.0.1-64`

#### Fortran benchmarks:
- `-w` `-m64` `-Wl,-z,-m64,` `muldefs` `-xCORE-AVX512` `-O3` `-ipo` `-no-prec-div`
- `-qopt-prefetch` `-ffinite-math-only`
- `-qopt-multiple-gather-scatter-by-shuffles` `-qopt-mem-layout-trans=4`
- `-nostandard-realloc-lhs` `-align array32byte`
- `-mbranches-within-32B-boundaries` `-ljemalloc` `-L/home/cpu2017/je5.0.1-64`

#### Benchmarks using both Fortran and C:
- `-w` `-m64` `-std=c11` `-Wl,-z,-m64,` `muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math`
- `-flto` `-mfpmath=sse` `-funroll-loops` `-qopt-mem-layout-trans=4` `-O3` `-ipo`
- `-no-prec-div` `-qopt-prefetch` `-ffinite-math-only`
- `-qopt-multiple-gather-scatter-by-shuffles`
- `-mbranches-within-32B-boundaries` `-nostandard-realloc-lhs`
- `-align array32byte` `-ljemalloc` `-L/home/cpu2017/je5.0.1-64`

#### Benchmarks using both C and C++:
- `-w` `-m64` `-std=c11` `-Wl,-z,-m64,` `muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math`
- `-flto` `-mfpmath=sse` `-funroll-loops` `-qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries` `-ljemalloc` `-L/home/cpu2017/je5.0.1-64`

#### Benchmarks using Fortran, C, and C++:
- `-w` `-m64` `-std=c11` `-Wl,-z,-m64,` `muldefs` `-xCORE-AVX512` `-Ofast` `-ffast-math`
- `-flto` `-mfpmath=sse` `-funroll-loops` `-qopt-mem-layout-trans=4` `-O3`
- `-no-prec-div` `-qopt-prefetch` `-ffinite-math-only`
- `-qopt-multiple-gather-scatter-by-shuffles`
- `-mbranches-within-32B-boundaries` `-nostandard-realloc-lhs`

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Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4310, 2.10GHz)

SPEC CPU®2017 Floating Point Rate Result

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SPECrate®2017_fp_base = 207
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
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Tested by: Cisco Systems

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Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
-align array32byte -ljemalloc -L/home/cpu2017/je5.0.1-64

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revl.xml

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