## Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4314, 2.40GHz)

<table>
<thead>
<tr>
<th>SPEC CPU®2017_int_base = 235</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak = Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Dec-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Sep-2021</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Sep-2021</td>
</tr>
</tbody>
</table>

### Hardware

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base (235)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perbench_r 64</td>
<td>502.gcc_r 64</td>
</tr>
<tr>
<td></td>
<td>197</td>
</tr>
</tbody>
</table>

### Software

<table>
<thead>
<tr>
<th>OS:</th>
<th>SUSE Linux Enterprise Server 15 SP2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++ Compiler Build 20210924 for Linux; Fortran: Version 2021.4.0 of Intel Fortran Compiler Classic Build 20210910 for Linux;</td>
</tr>
<tr>
<td>Parallel:</td>
<td>No</td>
</tr>
<tr>
<td>Firmware:</td>
<td>Version 5.0.1d released Aug-2021</td>
</tr>
<tr>
<td>File System:</td>
<td>btrfs</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>Power Management:</td>
<td>BIOS and OS set to prefer performance at the cost of additional power usage</td>
</tr>
</tbody>
</table>

### CPU Name: Intel Xeon Silver 4314  
**Max MHz:** 3400  
**Nominal:** 2400  
**Enabled:** 32 cores, 2 chips, 2 threads/core  
**Orderable:** 1.2 Chips  
**Cache L1:** 32 KB I + 48 KB D on chip per core  
**L2:** 1.25 MB I+D on chip per core  
**L3:** 24 MB I+D on chip per chip  
**Other:** None  
**Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)  
**Storage:** 1 x 240 GB M.2 SSD SATA  
**Other:** None  

---

**Hardware**

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- **Peak Pointers:** Not Applicable  
- **Other:** None  
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Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4314, 2.40GHz)

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<tr>
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<td>656</td>
<td>155</td>
<td>648</td>
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<td>502.gcc_r</td>
<td>64</td>
<td>459</td>
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<td>527</td>
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<td>525.x264_r</td>
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<td>531.deepsjeng_r</td>
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<td>548.exchange2_r</td>
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<td>557.xz_r</td>
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<td>528</td>
<td>131</td>
</tr>
</tbody>
</table>

SPECrate®2017_int_base = 235
SPECrate®2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/intel/tbb/2021.4.0/env/..lib/intel64/gcc4.8:/home/intel/mpi/2011.4.0/libfabric/lib:/home/intel/mpi/2011.4.0/lib/release:/home/intel/mpi/2011.4.0/lib:/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin:/home/intel/compiler/2021.4.0/linux/lib:/home/intel/click/2021.4.0/lib/intel64:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4314, 2.40GHz)

SPECrated®2017_int_base = 235
SPECrated®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

General Notes (Continued)

Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55b69a76f0e16accfc64d
running on perf-blade3 Thu Dec 9 16:11:12 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit

(Continued on next page)
Cisco Systems
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SPECRate®2017_int_base = 235
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

| Test Date: | Dec-2021 |
| Hardware Availability: | Sep-2021 |
| Software Availability: | Sep-2021 |

Platform Notes (Continued)

Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
Stepping: 6
CPU MHz: 3281.182
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 24576K
NUMA node0 CPU(s): 0-7, 32-39
NUMA node1 CPU(s): 8-15, 40-47
NUMA node2 CPU(s): 16-23, 48-55
NUMA node3 CPU(s): 24-31, 56-63
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pdcm dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault ebpx cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqrm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha尼 avx512bw avx512vl xsavesopt xsaveopt xsaves xsavecl xsavecl xsaveq ccmqแชสs cmmqb _total ccmqѿ_k_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vmbi umip pku ospe avx512_vbmi2 gfnl vaes vpcmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

/proc/cpuinfo cache data

Cache size : 24576 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)

(Continued on next page)
Cisco Systems
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<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>235</th>
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<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Date:** Dec-2021  
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**Tested by:** Cisco Systems  
**Hardware Availability:** Sep-2021  
**Software Availability:** Sep-2021

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**Platform Notes (Continued)**

```plaintext
node 0 cpus: 0 1 2 3 4 5 6 7 32 33 34 35 36 37 38 39
node 0 size: 515685 MB
node 0 free: 515353 MB
node 1 cpus: 8 9 10 11 12 13 14 15 40 41 42 43 44 45 46 47
node 1 size: 516057 MB
node 1 free: 515777 MB
node 2 cpus: 16 17 18 19 20 21 22 23 48 49 50 51 52 53 54 55
node 2 size: 516091 MB
node 2 free: 515831 MB
node 3 cpus: 24 25 26 27 28 29 30 31 56 57 58 59 60 61 62 63
node 3 size: 516088 MB
node 3 free: 515709 MB
node distances:
  node 0 1 2 3
  0: 10 11 20 20
  1: 11 10 20 20
  2: 20 20 10 11
  3: 20 20 11 10

From /proc/meminfo
MemTotal:       2113458076 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux perf-blade3 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
```

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4314, 2.40GHz)

SPECrater®2017_int_base = 235
SPECrater®2017_int_peak = Not Run

---

**Platform Notes (Continued)**

<table>
<thead>
<tr>
<th>CVE-2017-5754 (Meltdown):</th>
<th>Not affected</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVE-2018-3639 (Speculative Store Bypass):</td>
<td>Mitigation: Speculative Store Bypass disabled via prctl and seccomp</td>
</tr>
<tr>
<td>CVE-2017-5753 (Spectre variant 1):</td>
<td>Mitigation: usercopy/swaps barriers and __user pointer sanitization</td>
</tr>
<tr>
<td>CVE-2017-5715 (Spectre variant 2):</td>
<td>Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling</td>
</tr>
<tr>
<td>CVE-2020-0543 (Special Register Buffer Data Sampling):</td>
<td>Not affected</td>
</tr>
<tr>
<td>CVE-2019-11135 (TSX Asynchronous Abort):</td>
<td>Not affected</td>
</tr>
</tbody>
</table>

run-level 3 Dec 9 16:01

SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda2</td>
<td>btrfs</td>
<td>222G</td>
<td>60G</td>
<td>162G</td>
<td>27%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

<table>
<thead>
<tr>
<th>Vendor:</th>
<th>Cisco Systems Inc</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product:</td>
<td>UCSX-210C-M6</td>
</tr>
<tr>
<td>Serial:</td>
<td>FCH25057ALS</td>
</tr>
</tbody>
</table>

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:

<table>
<thead>
<tr>
<th>BIOS Vendor:</th>
<th>Cisco Systems, Inc.</th>
</tr>
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<tbody>
<tr>
<td>BIOS Version:</td>
<td>X210M6.5.0.id.0.0816211754</td>
</tr>
<tr>
<td>BIOS Date:</td>
<td>08/16/2021</td>
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<tr>
<td>BIOS Revision:</td>
<td>5.22</td>
</tr>
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(End of data from sysinfo program)

---

**Compiler Version Notes**

==============================================================================
| C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) 525.x264_r(base) 557.xz_r(base) |
|---------|-----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924

(Continued on next page)
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SPEC CPU®2017 Integer Rate Result
Copyright 2017-2022 Standard Performance Evaluation Corporation

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Compiler Version Notes (Continued)
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

--------------------------------------------------------------------------------
C++     | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
        | 541.leela_r(base)
--------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

--------------------------------------------------------------------------------
Fortran | 548.exchange2_r(base)
--------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

--------------------------------------------------------------------------------
Base Compiler Invocation
C benchmarks:
icx
C++ benchmarks:
icpx
Fortran benchmarks:
ifort

--------------------------------------------------------------------------------
Base Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
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Base Optimization Flags

C benchmarks:
- -W -std=c11 -m64 -Wl, -z, muldefs -xCORE-AVX512 -O3 -ffast-math
- -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- -mbranches-within-32B-boundaries
- -L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin
- -lqkmalloc

C++ benchmarks:
- -W -m64 -Wl, -z, muldefs -xCORE-AVX512 -O3 -ffast-math -flto
- -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- -mbranches-within-32B-boundaries
- -L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin
- -lqkmalloc

Fortran benchmarks:
- -W -m64 -Wl, -z, muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
- -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- -mbranches-within-32B-boundaries
- -L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin
- -lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revl.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-12-09 19:11:11-0500.
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