### Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)

**SPECrater®2017_int_base** = 148

**SPECrater®2017_int_peak** = Not Run

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<td>523.xalancbmk_r 40</td>
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<td>541.leela_r 40</td>
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<td>286</td>
</tr>
<tr>
<td>557.xz_r 40</td>
<td>81.6</td>
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</table>

### Hardware

**CPU Name:** Intel Xeon Silver 4310T

**Max MHz:** 3400

**Nominal:** 2300

Enabled: 20 cores, 2 chips, 2 threads/core

Orderable: 1.2 Chips

Cache L1: 32 KB I + 48 KB D on chip per core

Cache L2: 1.25 MB I+D on chip per core

Cache L3: 15 MB I+D on chip per chip

Other: None

Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)

Storage: 1 x 240 GB M.2 SSD SATA

Other: None

### Software

**OS:** SUSE Linux Enterprise Server 15 SP2

**Compiler:** C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++ Compiler Build 20210924 for Linux;

Fortran: Version 2021.4.0 of Intel Fortran Classic Build 20210910 for Linux;

**Parallel:** No

**Firmware:** Version 5.0.1d released Aug-2021

**File System:** btrfs

**System State:** Run level 3 (multi-user)

**Base Pointers:** 64-bit

**Peak Pointers:** Not Applicable

**Other:** None

**Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
### Results Table

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</tbody>
</table>

**SPECrate®2017_int_base = 148**

**SPECrate®2017_int_peak = Not Run**

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH =
"/home/intel/tbb/2021.4.0/env/..lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/libfabric/lib:/home/intel/mpi/2021.4.0/lib/release:/home/intel/mpi/2021.4.0/lib:/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64/_lin:/home/intel/compiler/2021.4.0/linux/lib:/home/intel/clck/2021.4.0/lib/intel64:/home/cpu2017/je5.0.1-32"

MALLOCONF = "retain:true"
```

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM

memory using openSUSE Leap 15.2

Transparent Huge Pages enabled by default

Prior to runcpu invocation

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)

**SPEC CPU®2017 Integer Rate Result**

<table>
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<th>SPECrate®2017_int_base</th>
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<table>
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<th>CPU2017 License</th>
<th>9019</th>
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<tbody>
<tr>
<td>Test Sponsor</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by</td>
<td>Cisco Systems</td>
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<tr>
<td>Test Date</td>
<td>Dec-2021</td>
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<tr>
<td>Hardware Availability</td>
<td>Sep-2021</td>
</tr>
<tr>
<td>Software Availability</td>
<td>Sep-2021</td>
</tr>
</tbody>
</table>

### General Notes (Continued)

Filesystem page cache synced and cleared with:
```bash
sync; echo 3> /proc/sys/vm/drop_caches
```
```
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

**BIOS Settings:**
- Adjacent Cache Line Prefetcher set to Disabled
- DCU Streamer Prefetch set to Disabled
- Sub NUMA Clustering set to Enabled
- LLC Dead Line set to Disabled
- Memory Refresh Rate set to 1x Refresh
- ADDDC Sparing set to Disabled
- Patrol Scrub set to Disabled
- Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on perf-blade5 Fri Dec 10 11:40:31 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
```bash
model name : Intel(R) Xeon(R) Silver 4310T CPU @ 2.30GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 5 6 7 8 9
physical 1: cores 0 1 2 3 4 5 6 7 8 9
```

From lscpu from util-linux 2.33.1:
```bash
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
```

(Continued on next page)
Cisco Systems  
Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)  

SPECrate®2017_int_base = 148  
SPECrate®2017_int_peak = Not Run

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Test Date: Dec-2021  
Tested by: Cisco Systems  
Hardware Availability: Sep-2021  
Software Availability: Sep-2021

Platform Notes (Continued)

Address sizes: 46 bits physical, 57 bits virtual  
CPU(s): 40  
On-line CPU(s) list: 0-39  
Thread(s) per core: 2  
Core(s) per socket: 10  
Socket(s): 2  
NUMA node(s): 2  
Vendor ID: GenuineIntel  
CPU family: 6  
Model: 106  
Model name: Intel(R) Xeon(R) Silver 4310T CPU @ 2.30GHz  
Stepping: 6  
CPU MHz: 2101.999  
CPU max MHz: 3400.0000  
CPU min MHz: 800.0000  
BogoMIPS: 4600.00  
Virtualization: VT-x  
L1d cache: 48K  
L1i cache: 32K  
L2 cache: 1280K  
L3 cache: 15360K  
NUMA node0 CPU(s): 0-9,20-29  
NUMA node1 CPU(s): 10-19,30-39  
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdrtsc lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtses64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_l3 invvpcid_single ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw avx512vl xsxveopt xsaveopt xsavec xsaveopt xsaves cmq_llc cmq_occmap llc cmq_mbb_total cmq_mbb_local wbinvd dtcer dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vmbi umip pku ospe avx512_vmbi2 gfnv vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_lid arch_capabilities

From numactl --hardware  
WARNING: a numactl 'node' might or might not correspond to a physical chip.  
available: 2 nodes (0-1)  
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29  
node 0 size: 1031746 MB  
node 0 free: 1031224 MB

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)  

**SPEC CPU®2017 Integer Rate Result**

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 148</th>
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<tbody>
<tr>
<td>SPECrate®2017_int_peak = Not Run</td>
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</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Platform Notes (Continued)**

- **node 1 cpus:** 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
- **node 1 size:** 1032183 MB
- **node 1 free:** 1031711 MB
- **node distances:**
  - 0: 10 20
  - 1: 20 10

From `/proc/meminfo`

- **MemTotal:** 2113464140 kB
- **HugePages_Total:** 0
- **Hugepagesize:** 2048 kB

From `/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor`

- `has performance`

From `/etc/*release*` /`/etc/*version*`

- `os-release:`
  - `NAME="SLES"
  - `VERSION="15-SP2"
  - `VERSION_ID="15.2"
  - `PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
  - `ID="sles"
  - `ID_LIKE="suse"
  - `ANSI_COLOR="0;32"
  - `CPE_NAME="cpe:/o:suse:sles:15:sp2"

`uname -a:`

- Linux perf-blade5 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba)  
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

- **CVE-2018-12207 (iTLB Multihit):** Not affected
- **CVE-2018-3620 (L1 Terminal Fault):** Not affected
- **Microarchitectural Data Sampling:** Not affected
- **CVE-2017-5754 (Meltdown):** Not affected
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: usercopy/swaps barriers and __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- **CVE-2020-0543 (Special Register Buffer Data Sampling):** Not affected
- **CVE-2019-11135 (TSX Asynchronous Abort):** Not affected

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPEC CPU®2017 Integer Rate Result

SPECrates®2017_int_base = 148
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Platform Notes (Continued)

run-level 3 Dec 10 11:33

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb2 btrfs 224G 52G 172G 24% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSX-210C-M6
Serial: FCH250671LG

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: X210M6.5.0.1d.0.0816211754
BIOS Date: 08/16/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

C
500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
525.x264_r(base) 557.xz_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

C++
520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
541.leela_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
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(Continued on next page)
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Compiler Version Notes (Continued)

Fortran | 548.exchange2_r(base)  
-----------------------------------------------------------------  
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.4.0 Build 20210910_000000  
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.  
-----------------------------------------------------------------

Base Compiler Invocation

C benchmarks:  
icx

C++ benchmarks:  
icpx

Fortran benchmarks:  
ifort

Base Portatility Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.ommnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:  
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math  
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4  
-mbranches-within-32B-boundaries  
-L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin  
-lqkmalloc

(Continued on next page)
# SPEC CPU®2017 Integer Rate Result

Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Silver 4310T, 2.30GHz)

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**Test Date:** Dec-2021  
**Hardware Availability:** Sep-2021  
**Software Availability:** Sep-2021

## Base Optimization Flags (Continued)

**C++ benchmarks:**
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto  
-mfpmath=sse -funroll-loops -g -ipo -no-prec-div  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
-mbranches-within-32B-boundaries  
-L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin  
-lqkmalloc

**Fortran benchmarks:**
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
-mbranches-within-32B-boundaries  
-L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin  
-lqkmalloc

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Spec CPU®2017 v1.1.8 tested on 2021-12-10 14:40:30-0500.  
Originally published on 2022-01-04.