## SPEC CPU®2017 Integer Rate Result

### Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Silver 4316, 2.30GHz)

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base = 282</th>
<th>SPECrate®2017_int_peak = Not Run</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>80</td>
<td>190</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>80</td>
<td>233</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>80</td>
<td>489</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>80</td>
<td>357</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>80</td>
<td>578</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>80</td>
<td>211</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>80</td>
<td>202</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>80</td>
<td>551</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>80</td>
<td>158</td>
</tr>
</tbody>
</table>

---

### Hardware

- **CPU Name:** Intel Xeon Silver 4316
- **Max MHz:** 3400
- **Nominal:** 2300
- **Enabled:** 40 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:**
  - I: 32 KB on chip per core
  - D: 48 KB on chip per core
- **Cache L2:**
  - 1.25 MB I+D on chip per core
- **Cache L3:**
  - 30 MB I+D on chip per chip
- **Other:** None
- **Memory:** 1 TB (32 x 32 GB 2Rx4 PC4-3200AA-R, running at 2666)
- **Storage:** 1 x 240 GB M.2 SSD SATA
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
- **Compiler:**
  - C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++ Compiler Build 20210924 for Linux;
  - Fortran: Version 2021.4.0 of Intel Fortran Classic Build 20210910 for Linux;
- **Parallel:** No
- **Firmware:** Version 5.0.1d released Aug-2021
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
## Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4316, 2.30GHz)

### SPECrate®2017_int_base = 282
### SPECrate®2017_int_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Dec-2021  
**Hardware Availability:** Sep-2021  
**Software Availability:** Sep-2021

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>80</td>
<td>671</td>
<td>190</td>
<td>669</td>
<td>190</td>
<td>671</td>
<td>190</td>
</tr>
<tr>
<td>503.gcc_r</td>
<td>80</td>
<td>486</td>
<td>233</td>
<td>487</td>
<td>232</td>
<td>485</td>
<td>233</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>80</td>
<td>264</td>
<td>489</td>
<td><strong>265</strong></td>
<td><strong>489</strong></td>
<td>266</td>
<td>487</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>80</td>
<td>556</td>
<td>189</td>
<td>555</td>
<td>189</td>
<td>556</td>
<td>189</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>80</td>
<td>236</td>
<td>358</td>
<td>237</td>
<td>357</td>
<td>237</td>
<td>357</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>80</td>
<td>242</td>
<td>578</td>
<td>243</td>
<td>577</td>
<td>242</td>
<td>578</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>80</td>
<td>434</td>
<td>211</td>
<td>434</td>
<td>211</td>
<td>434</td>
<td>211</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>80</td>
<td>657</td>
<td>202</td>
<td>657</td>
<td>202</td>
<td>657</td>
<td>202</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>80</td>
<td>382</td>
<td>549</td>
<td>380</td>
<td>552</td>
<td>380</td>
<td>551</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>80</td>
<td>546</td>
<td>158</td>
<td><strong>546</strong></td>
<td><strong>158</strong></td>
<td>545</td>
<td>159</td>
</tr>
</tbody>
</table>

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
"/home/intel/tbb/2021.4.0/env/../lib/intel64/gcc4.8:/home/intel/mpi/2021  
.4.0/libfabric/lib:/home/intel/mpi/2021.4.0//lib/release:/home/intel/mp 
i/2021.4.0//lib:/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64 _lin:/home/intel/compiler/2021.4.0/linux/lib:/home/intel/clck/2021.4.0/l 
ib/intel64:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"
```

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM  
memory using openSUSE Leap 15.2  
Transparent Huge Pages enabled by default

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4316, 2.30GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2022 Standard Performance Evaluation Corporation

General Notes (Continued)

Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acfc64d
running on perf-blade6 Thu Dec 9 13:05:19 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4316, 2.30GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrates
SPECrates®2017_int_base = 282
SPECrates®2017_int_peak = Not Run

Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Platform Notes (Continued)

Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz
Stepping: 6
CPU MHz: 2896.281
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 30720K
NUMA node0 CPU(s): 0-9, 40-49
NUMA node1 CPU(s): 10-19, 50-59
NUMA node2 CPU(s): 20-29, 60-69
NUMA node3 CPU(s): 30-39, 70-79
Flags: fpu vme de pse tm mtrr pge mca cmov pat pse36 clflush dtc npx x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 3nowprefetch cpuid_fault epb cat_13

Warning: a numactl 'node' might or might not correspond to a physical chip.
From numactl --hardware

/proc/cpuinfo cache data

cache size: 30720 KB

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4316, 2.30GHz)

| SPECrate®2017_int_base = 282 |
| SPECrate®2017_int_peak = Not Run |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Platform Notes (Continued)

node 0 cpus: 0 1 2 3 4 5 6 7 8 9 40 41 42 43 44 45 46 47 48 49
node 0 size: 257603 MB
node 0 free: 257279 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 50 51 52 53 54 55 56 57 58 59
node 1 size: 258043 MB
node 1 free: 257678 MB
node 2 cpus: 20 21 22 23 24 25 26 27 28 29 60 61 62 63 64 65 66 67 68 69
node 2 size: 258043 MB
node 2 free: 257777 MB
node 3 cpus: 30 31 32 33 34 35 36 37 38 39 70 71 72 73 74 75 76 77 78 79
node 3 size: 258039 MB
node 3 free: 257728 MB
node distances:
node 0 1 2 3
0: 10 11 20 20
1: 11 10 20 20
2: 20 20 10 11
3: 20 20 11 10

From /proc/meminfo
MemTotal: 1056490408 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux perf-blade6 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba)x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4316, 2.30GHz)

SPECratenew_int_base = 282
SPECratenew_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Platform Notes (Continued)

CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Dec 9 12:58
SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 222G 41G 181G 19% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSX-210C-M6
Serial: FCH25057ANW

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: X210M6.5.0.1d.0.0816211754
BIOS Date: 08/16/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

================================reich
C   500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
   525.x264_r(base) 557.xz_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4316, 2.30GHz)

| SPECrate®2017_int_base = 282 |
| SPECrate®2017_int_peak = Not Run |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
 Tested by: Cisco Systems

Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Compiler Version Notes (Continued)

Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

---

C++ | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base) 541.leela_r(base)
---

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
---

Fortran | 548.exchange2_r(base)
---

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
---

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
## SPEC CPU®2017 Integer Rate Result

### Cisco Systems

**Cisco UCS X210c M6 (Intel Xeon Silver 4316, 2.30GHz)**

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Dec-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Sep-2021</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Sep-2021</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base =** 282

**SPECrate®2017_int_peak =** Not Run

### Base Optimization Flags

**C benchmarks:**
- `-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math`
- `-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries`
- `-L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

**C++ benchmarks:**
- `-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto`
- `-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries`
- `-L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

**Fortran benchmarks:**
- `-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div`
- `-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`
- `-mbranches-within-32B-boundaries`
- `-L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

---

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-12-09 16:05:18-0500.
Originally published on 2022-01-04.