Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Silver 4316, 2.30GHz)

SPECrates:
- **SPECrates**\textsuperscript{2017}\textunderscore fp\textunderscore base = 298
- **SPECrates**\textsuperscript{2017}\textunderscore fp\textunderscore peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
- **CPU Name**: Intel Xeon Silver 4316
- **Max MHz**: 3400
- **Nominal**: 2300
- **Enabled**: 40 cores, 2 chips, 2 threads/core
- **Orderable**: 1,2 Chips
- **Cache L1**: 32 KB I + 48 KB D on chip per core
- **L2**: 1.25 MB I+D on chip per core
- **L3**: 30 MB I+D on chip per chip
- **Memory**: 1 TB (32 x 32 GB 2Rx4 PC4-3200AA-R, running at 2666)
- **Storage**: 1 x 240 GB M.2 SSD SATA
- **Other**: None

Software
- **OS**: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
- **Compiler**: C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++ Compiler Build 20210924 for Linux;
  Fortran: Version 2021.4.0 of Intel Fortran Compiler Classic Build 20210910 for Linux;
- **Parallel**: No
- **Firmware**: Version 5.0.1d released Aug-2021
- **File System**: btrfs
- **System State**: Run level 3 (multi-user)
- **Base Pointers**: 64-bit
- **Peak Pointers**: Not Applicable
- **Other**: jemalloc memory allocator V5.0.1
- **Power Management**: BIOS and OS set to prefer performance at the cost of additional power usage
### RESULTS TABLE

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>80</td>
<td>1328</td>
<td>604</td>
<td>1329</td>
<td>604</td>
<td>1326</td>
<td>605</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>80</td>
<td>260</td>
<td>389</td>
<td>259</td>
<td>391</td>
<td>260</td>
<td>390</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>80</td>
<td>371</td>
<td>205</td>
<td>371</td>
<td>205</td>
<td>370</td>
<td>205</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>80</td>
<td>1321</td>
<td>158</td>
<td>1334</td>
<td>157</td>
<td>1315</td>
<td>159</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>80</td>
<td>597</td>
<td>313</td>
<td>598</td>
<td>312</td>
<td>597</td>
<td>313</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>80</td>
<td>394</td>
<td>214</td>
<td>396</td>
<td>213</td>
<td>395</td>
<td>213</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>80</td>
<td>653</td>
<td>274</td>
<td>653</td>
<td>274</td>
<td>656</td>
<td>273</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>80</td>
<td>363</td>
<td>335</td>
<td>362</td>
<td>336</td>
<td>363</td>
<td>336</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>80</td>
<td>490</td>
<td>286</td>
<td>490</td>
<td>286</td>
<td>490</td>
<td>286</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>80</td>
<td>243</td>
<td>817</td>
<td>255</td>
<td>781</td>
<td>243</td>
<td>819</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>80</td>
<td>237</td>
<td>569</td>
<td>236</td>
<td>569</td>
<td>236</td>
<td>570</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>80</td>
<td>1647</td>
<td>189</td>
<td>1647</td>
<td>189</td>
<td>1648</td>
<td>189</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>80</td>
<td>1013</td>
<td>126</td>
<td>1017</td>
<td>125</td>
<td>1010</td>
<td>126</td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base = 298**

**SPECrate®2017_fp_peak = Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
"/home/intel/tbb/2021.4.0/env/../lib/intel64/gcc4.8:/home/intel/mpi/2021 
.4.0/libfabric/lib:/home/intel/mpi/2021.4.0/lib/release:/home/intel/mpi 
1/2021.4.0/lib:/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64 
_lin:/home/intel/compiler/2021.4.0/linux/lib:/home/intel/clck/2021.4.0/l 
ib/intel64:/home/cpu2017/je5.0.1-32"
```

```
MALLOC_CONF = "retain:true"
```

---

Cisco Systems
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---

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Hardware Availability: Sep-2021
Software Availability: Sep-2021
Test Date: Dec-2021
Tested by: Cisco Systems
Test Sponsor: Cisco Systems
Hardware Availability: Sep-2021
Software Availability: Sep-2021

---

SPEC CPU®2017 Floating Point Rate Result
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Cisco UCS X210c M6 (Intel Xeon Silver 4316, 2.30GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2022 Standard Performance Evaluation Corporation

SPEC CPU 2017 Floating Point Rate Result

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General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDC Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on perf-blade6 Thu Dec 9 17:10:27 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40

(Continued on next page)
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Software Availability: Sep-2021

Platform Notes (Continued)

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

From lscpu from util-linux 2.33.1:

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz
Stepping: 6
CPU MHz: 800.346
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 30720K
NUMA node0 CPU(s): 0-9,40-49
NUMA node1 CPU(s): 10-19,50-59
NUMA node2 CPU(s): 20-29,60-69
NUMA node3 CPU(s): 30-39,70-79
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrp pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd
mba ibrs ibbp stibp ibrs_enhanced tpr_shadow vni_flexpriority ept vpid ept_ad
fsqm vbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpccd rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occump_llc cqm_mbb_total
cqmm_mbb_local wbnoivd dtherm ida arat pln pts hwp hwpt_act_window hwp_epp
hwp_pkg_req avx512vmbi umip pku ospke avx512_vmbi2 gfn vaes vpcmlqdq avx512_vnmi
avx512_bitalg tme avx512 vpoptndq la57 rpdpid md_clear pconfig flush_lld
arch_capabilities

(Continued on next page)
Platform Notes (Continued)

/proc/cpuinfo cache data
  cache size : 30720 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 40 41 42 43 44 45 46 47 48 49
  node 0 size: 257637 MB
  node 0 free: 257255 MB
  node 1 cpus: 10 11 12 13 14 15 16 17 18 19 50 51 52 53 54 55 56 57 58 59
  node 1 size: 258043 MB
  node 1 free: 257721 MB
  node 2 cpus: 20 21 22 23 24 25 26 27 28 29 60 61 62 63 64 65 66 67 68 69
  node 2 size: 258099 MB
  node 2 free: 257679 MB
  node 3 cpus: 30 31 32 33 34 35 36 37 38 39 70 71 72 73 74 75 76 77 78 79
  node 3 size: 258039 MB
  node 3 free: 257769 MB
  node distances:
  node   0   1   2   3
  0:  10  11  20  20
  1:  11  10  20  20
  2:  20  20  10  11
  3:  20  20  11  10

From /proc/meminfo
  MemTotal:       1056490408 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

  uname -a:
    Linux perf-blade6 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba)
    x86_64 x86_64 x86_64 GNU/Linux

(Continued on next page)
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SPEC®2017_fp_base = 298
SPEC®2017_fp_peak = Not Run

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Hardware Availability: Sep-2021  
Tested by: Cisco Systems  
Software Availability: Sep-2021  
Test Date: Dec-2021

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,</td>
<td></td>
</tr>
<tr>
<td>Version 2021.4.0 Build 20210924</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2021 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>-------</td>
<td>-----------------------------------------------------</td>
</tr>
<tr>
<td>C++</td>
<td>508.namd_r(base) 510.parest_r(base)</td>
</tr>
<tr>
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<td>-----------------------------------------------------</td>
</tr>
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<td></td>
</tr>
<tr>
<td>-------</td>
<td>-----------------------------------------------------</td>
</tr>
<tr>
<td>C++, C</td>
<td>511.povray_r(base) 526.blender_r(base)</td>
</tr>
<tr>
<td>-------</td>
<td>-----------------------------------------------------</td>
</tr>
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<td></td>
</tr>
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</tr>
<tr>
<td>-------</td>
<td>-----------------------------------------------------</td>
</tr>
<tr>
<td>C++, C, Fortran</td>
<td>507.cactuBSSN_r(base)</td>
</tr>
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<td>-----------------------------------------------------</td>
</tr>
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<td></td>
</tr>
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<td></td>
</tr>
<tr>
<td>Version 2021.4.0 Build 20210924</td>
<td></td>
</tr>
<tr>
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<td></td>
</tr>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on</td>
<td></td>
</tr>
<tr>
<td>Intel(R) 64, Version 2021.4.0 Build 20210910_000000</td>
<td></td>
</tr>
<tr>
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<td></td>
</tr>
<tr>
<td>-------</td>
<td>-----------------------------------------------------</td>
</tr>
<tr>
<td>Fortran</td>
<td>503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)</td>
</tr>
<tr>
<td>-------</td>
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</tr>
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<td></td>
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<td></td>
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SPECrater®2017_fp_base = 298
SPECrater®2017_fp_peak = Not Run
Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Compiler Version Notes (Continued)
==============================================================================
Fortran, C | 521.wrf_r(base) 527.cam4_r(base)
-----------------------------------------------------------------------------
Intel (R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
Base Compiler Invocation
C benchmarks:
icx
C++ benchmarks:
icpx
Fortran benchmarks:
ifort
Benchmarks using both Fortran and C:
ifort icx
Benchmarks using both C and C++:
icpx icx
Benchmarks using Fortran, C, and C++:
icpx icx ifort
Base Portability Flags
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
(Continued on next page)
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Base Portability Flags (Continued)

527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
- w -std=c11 -m64 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math
- f1to -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

C++ benchmarks:
- w -m64 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math -f1to
- mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

Fortran benchmarks:
- w -m64 -Wl,-z,-muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
- qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
- nostandard-realloc-lhs -align array32byte
- mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

Benchmarks using both Fortran and C:
- w -m64 -std=c11 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math
- f1to -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
- no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles
- mbranches-within-32B-boundaries -nostandard-realloc-lhs
- align array32byte -ljemalloc -L/home/cpu2017/je5.0.1-64

Benchmarks using both C and C++:
- w -m64 -std=c11 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math
- f1to -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

Benchmarks using Fortran, C, and C++:
- w -m64 -std=c11 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math
- f1to -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
- no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles
- mbranches-within-32B-boundaries -nostandard-realloc-lhs

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**SPEC CPU 2017 Floating Point Rate Result**

**SPECrate®2017_fp_base = 298**
**SPECrate®2017_fp_peak = Not Run**

Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
- `align array32byte -ljemalloc -L/home/cpu2017/je5.0.1-64`

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links: