## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**

Cisco UCS X210c M6 (Intel Xeon Platinum 8352M, 2.30GHz)

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Date</th>
<th>Test Sponsor</th>
<th>Hardware Availability</th>
<th>Tested by</th>
<th>Software Availability</th>
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<tr>
<td>9019</td>
<td>Dec-2021</td>
<td>Cisco Systems</td>
<td>Sep-2021</td>
<td>Cisco Systems</td>
<td>Sep-2021</td>
</tr>
</tbody>
</table>

### SPECspeed®2017_int_base = 11.8

**SPECspeed®2017_int_peak = Not Run**

### Hardware

- **CPU Name:** Intel Xeon Platinum 8352M
- **Max MHz:** 3500
- **Nominal:** 2300
- **Enabled:** 64 cores, 2 chips
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **L2:** 1.25 MB I+D on chip per core
- **L3:** 48 MB I+D on chip per chip
- **Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
- **Storage:** 1 x 240 GB M.2 SSD SATA
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
- **Compiler:** C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++ Compiler Build 20210924 for Linux; Fortran: Version 2021.4.0 of Intel Fortran Compiler Classic Build 20210910 for Linux;
- **Parallel:** Yes
- **Firmware:** Version 5.0.1d released Aug-2021
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage

### Results

<table>
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<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
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<tbody>
<tr>
<td>600.perlbench_s</td>
<td>64</td>
<td>10.9</td>
<td>Not Run</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>64</td>
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<td>64</td>
<td>13.3</td>
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</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>64</td>
<td>5.92</td>
<td></td>
</tr>
<tr>
<td>625.x264_s</td>
<td>64</td>
<td>4.77</td>
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<tr>
<td>631.deepsjeng_s</td>
<td>64</td>
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<tr>
<td>648.exchange2_s</td>
<td>64</td>
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<tr>
<td>657.xz_s</td>
<td>64</td>
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Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Platinum 8352M, 2.30GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
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<th>Seconds</th>
<th>Ratio</th>
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</table>

SPECspeed®2017_int_base = 11.8
SPECspeed®2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/intel/tbb/2021.4.0/env/../lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:/home/intel/mpi/2021.4.0/lib/intel64/gcc4.8:
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2

(Continued on next page)
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General Notes (Continued)

Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Intel Hyper-Threading Technology set to Disable
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acfc64d
running on perf-blade6 Thu Dec 16 08:14:38 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8352M CPU @ 2.30GHz
  2 "physical id"'s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 32
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

(Continued on next page)
# Platform Notes (Continued)

25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

From lscpu from util-linux 2.33.1:

- **Architecture:** x86_64
- **CPU op-mode(s):** 32-bit, 64-bit
- **Byte Order:** Little Endian
- **Address sizes:** 46 bits physical, 57 bits virtual
- **CPU(s):** 64
- **On-line CPU(s) list:** 0-63
- **Thread(s) per core:** 1
- **Core(s) per socket:** 32
- **Socket(s):** 2
- **NUMA node(s):** 2
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 106
- **Model name:** Intel(R) Xeon(R) Platinum 8352M CPU @ 2.30GHz
- **Stepping:** 6
- **CPU MHz:** 3224.246
- **CPU max MHz:** 3500.0000
- **CPU min MHz:** 800.0000
- **BogoMIPS:** 4600.00
- **Virtualization:** VT-x
- **L1d cache:** 48K
- **L1i cache:** 32K
- **L2 cache:** 1280K
- **L3 cache:** 49152K
- **NUMA node0 CPU(s):** 0-31
- **NUMA node1 CPU(s):** 32-63

**Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrnr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invvpdcid_single ssbd mbs rdp old ibrs ibrd ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ibrms invocation rdmsi rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsavevc xSAVE xsvave cqm_lll cqm_occup llc cqm_mbm_total cqm_mbb_local wbnoivd dtherm iida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_reg avx512vbi umip pku ospke avx512_vbmi2 gfn vaes vpclmlqdq avx512_vnni avx512_bbitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_lld arch_capabilities

/proc/cpuinfo cache data

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## Cisco Systems
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### SPEC CPU®2017 Integer Speed Result

**SPECspeed®2017_int_base = 11.8**

**SPECspeed®2017_int_peak = Not Run**

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### Platform Notes (Continued)

```
cache size : 49152 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 0 size: 1031777 MB
node 0 free: 1031207 MB
node 1 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
node 1 size: 1032146 MB
node 1 free: 1031571 MB
node distances:
node   0   1
0:  10  20
1:  20  10

From /proc/meminfo
MemTotal:       2113458552 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"
uname -a:
Linux perf-blade6 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
```

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SPECs speed® 2017_int_base = 11.8
SPECs speed® 2017_int_peak = Not Run

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Test Sponsor: Cisco Systems
Software Availability: Sep-2021

Platform Notes (Continued)

CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Dec 16 07:50

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 222G 41G 181G 19% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSX-210C-M6
Serial: FCH25057ANW

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: X210M6.5.0.1d.0.0816211754
BIOS Date: 08/16/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) | 625.x264_s(base) 657.xz_s(base)
==============================================================================

Intel(R) oneAPI DPC+/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

(Continued on next page)
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SPECs®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Compiler Version Notes (Continued)

==============================================================================
| C++ | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base) |
|     | 641.leela_s(base)     |

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

==============================================================================
| Fortran | 648.exchange2_s(base) |

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

==============================================================================

Base Compiler Invocation

C benchmarks:
icx
C++ benchmarks:
icpx
Fortran benchmarks:
ifort

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
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SPECspeed®2017_int_base = 11.8
SPECspeed®2017_int_peak = Not Run

Base Optimization Flags

C benchmarks:
-DSPEC_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/home/cpu2017/je5.0.1-64 -ljemalloc

C++ benchmarks:
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin/
-lqkmalloc

Fortran benchmarks:
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revl.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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