# SPEC CPU®2017 Floating Point Rate Result

## Hewlett Packard Enterprise

**Synergy 480 Gen10 Plus**  
(3.00 GHz, Intel Xeon Gold 5317)

### CPU2017 License: 3  
Test Sponsor: HPE  
Tested by: HPE  
Test Date: Dec-2021  
Hardware Availability: Nov-2021  
Software Availability: Dec-2020

### Hardware

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>228</td>
<td>234</td>
</tr>
</tbody>
</table>

### Benchmark Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>48</td>
<td>290</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>48</td>
<td>290</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>48</td>
<td>152</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>24</td>
<td>131</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>48</td>
<td>225</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>48</td>
<td>213</td>
</tr>
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<td>221</td>
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<td>179</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>48</td>
<td>152</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
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<td>152</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>24</td>
<td>152</td>
</tr>
</tbody>
</table>

### CPU Name: Intel Xeon Gold 5317  
Max MHz: 3600  
Nominal: 3000  
Enabled: 24 cores, 2 chips, 2 threads/core  
Orderable: 1, 2 chip(s)  
Cache L1: 32 KB I + 48 KB D on chip per core  
L2: 1.25 MB I+D on chip per core  
L3: 18 MB I+D on chip per chip  
Other: None  
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2933)  
Storage: 1 x 800 GB SAS SSD, RAID 0  
Other: None

### Software

| OS:  | Red Hat Enterprise Linux 8.3 (Ootpa)  
Kernel 4.18.0-240.el8.x86_64 |
<table>
<thead>
<tr>
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</tr>
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<tbody>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;</td>
</tr>
<tr>
<td>Firmware:</td>
<td>HPE BIOS Version I44 v1.54 11/03/2021 released Nov-2021</td>
</tr>
<tr>
<td>File System:</td>
<td>xfs</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Other:</td>
<td>jemalloc memory allocator V5.0.1</td>
</tr>
</tbody>
</table>

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

**Hewlett Packard Enterprise**  
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### Software (Continued)

*Power Management:* BIOS set to prefer performance at the cost of additional power usage

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Base Copies</th>
<th>Base Seconds</th>
<th>Base Ratio</th>
<th>Peak Copies</th>
<th>Peak Seconds</th>
<th>Peak Ratio</th>
</tr>
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<tr>
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<tr>
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<td>961</td>
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<tr>
<td>511.povray_r</td>
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<td>497</td>
<td>225</td>
<td>498</td>
<td>225</td>
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<tr>
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<td>105</td>
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<td>105</td>
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</table>

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

*Stack size set to unlimited using "ulimit -s unlimited"*

*Transparent Huge Pages enabled by default*

*Prior to runcpu invocation*

*Filesystem page cache synced and cleared with:*

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

### Environment Variables Notes

*Environment variables set by runcpu before the start of the run:*

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
```
## General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
memory using Red Hat Enterprise Linux 8.1
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Submitted by: "Bucek, James" <james.bucek@hpe.com>
Submitted: Wed Jan 12 10:02:51 EST 2022
Submission: cpu2017-20220103-30703.sub

## Platform Notes

BIOS Configuration:
Workload Profile set to General Throughput Compute
Memory Patrol Scrubbing set to Disabled
Advanced Memory Protection set to Advanced ECC
Last Level Cache (LLC) Prefetch set to Enabled
Last Level Cache (LLC) Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Thermal Configuration set to Maximum Cooling
Workload Profile set to Custom
  DCU Stream Prefetcher set to Disabled
  XPT Remote Prefetcher set to Enabled
  Energy/Performance Bias set to Balanced Performance

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on localhost.localdomain Sat Dec 11 10:17:31 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 5317 CPU @ 3.00GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following

(Continued on next page)
**Platform Notes (Continued)**

excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

<table>
<thead>
<tr>
<th>Field</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU cores</td>
<td>12</td>
</tr>
<tr>
<td>Siblings</td>
<td>24</td>
</tr>
<tr>
<td>Physical 0: cores</td>
<td>0 1 2 3 4 5 6 7 8 9 10 11</td>
</tr>
<tr>
<td>Physical 1: cores</td>
<td>0 1 2 3 4 5 6 7 8 9 10 11</td>
</tr>
</tbody>
</table>

From lscpu from util-linux 2.32.1:

- **Architecture**: x86_64
- **CPU op-mode(s)**: 32-bit, 64-bit
- **Byte Order**: Little Endian
- **CPU(s)**: 48
- **On-line CPU(s) list**: 0-47
- **Thread(s) per core**: 2
- **Core(s) per socket**: 12
- **Socket(s)**: 2
- **NUMA node(s)**: 4
- **Vendor ID**: GenuineIntel
- **CPU family**: 6
- **Model**: 106
- **Model name**: Intel(R) Xeon(R) Gold 5317 CPU @ 3.00GHz
- **Stepping**: 6
- **CPU MHz**: 2751.199
- **BogoMIPS**: 6000.00
- **Virtualization**: VT-x
- **L1d cache**: 48K
- **L1i cache**: 32K
- **L2 cache**: 1280K
- **L3 cache**: 18432K
- **NUMA node0 CPU(s)**: 0-5, 24-29
- **NUMA node1 CPU(s)**: 6-11, 30-35
- **NUMA node2 CPU(s)**: 12-17, 36-41
- **NUMA node3 CPU(s)**: 18-23, 42-47
- **Flags**: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb ibrs_enabled tpr_shadow vmi flexpriority ept pvd ept_ad fsdistbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushht apt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local split_lock_detect wbnoiwvd dtherm ida arat pni pts avx512v bmi umip pku ospke avx512_vbmi2 gfn vaes vclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

/proc/cpuinfo cache data

(Continued on next page)
Platform Notes (Continued)

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 24 25 26 27 28 29
node 0 size: 509276 MB
node 0 free: 515159 MB
node 1 cpus: 6 7 8 9 10 11 30 31 32 33 34 35
node 1 size: 509538 MB
node 1 free: 515651 MB
node 2 cpus: 12 13 14 15 16 17 36 37 38 39 40 41
node 2 size: 510210 MB
node 2 free: 515847 MB
node 3 cpus: 18 19 20 21 22 23 42 43 44 45 46 47
node 3 size: 510112 MB
node 3 free: 515756 MB
node distances:
node   0   1   2   3
0:  10  20  30  30
1:  20  10  30  30
2:  30  30  10  20
3:  30  30  20  10

From /proc/meminfo
MemTotal:       2113491180 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
/sbin/tuned-adm active
Current active profile: throughput-performance

From /etc/*release* /etc/*version*
os-release:
   NAME="Red Hat Enterprise Linux"
   VERSION="8.3 (Ootpa)"
   ID="rhel"
   ID_LIKE="fedora"
   VERSION_ID="8.3"
   PLATFORM_ID="platform:el8"
   PRETTY_NAME="Red Hat Enterprise Linux 8.3 (Ootpa)"
   ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.3:ga

uname -a:

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10 Plus
(3.00 GHz, Intel Xeon Gold 5317)

SPECrate®2017_fp_base = 228
SPECrate®2017_fp_peak = 234

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Dec-2021
Hardware Availability: Nov-2021
Software Availability: Dec-2020

Platform Notes (Continued)

Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Wed Sep 23 05:13:10 EDT 2020
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapsgs barriers and __user pointer sanitization
CVE-2017-5753 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2017-5715 (Spectre variant 2):
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Dec 11 10:16
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs 670G 111G 559G 17% /home

From /sys/devices/virtual/dmi/id
Vendor: HPE
Product: Synergy 480 Gen10 Plus
Product Family: Synergy
Serial: CN70330Q5F

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x Micron 36ASF8G72PZ-3G2B2 64 GB 2 rank 3200, configured at 2933

BIOS:
BIOS Vendor: HPE
BIOS Version: I44
BIOS Date: 11/03/2021
BIOS Revision: 1.54
Firmware Revision: 2.40

(End of data from sysinfo program)
**Compiler Version Notes**

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C

| 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak) |

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

C++

| 508.namd_r(base, peak) 510.parest_r(base, peak) |

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

C++, C

| 511.povray_r(peak) |

Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

C++, C

| 511.povray_r(base) 526.blender_r(base, peak) |

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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---

C++, C

| 511.povray_r(peak) |

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---

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| 511.povray_r(base) 526.blender_r(base, peak) |

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Compiler Version Notes (Continued)

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----------------------------------------
C++, C          | 511.povray_r(base) 526.blender_r(base, peak)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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C++, C, Fortran | 507.cactuBSSN_r(base, peak)
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Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
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SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2022 Standard Performance Evaluation Corporation

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10 Plus
(3.00 GHz, Intel Xeon Gold 5317)

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SPECrate®2017_fp_peak = 234

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Dec-2021
Hardware Availability: Nov-2021
Software Availability: Dec-2020

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64 507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64 510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64 519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-ffloat-math=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Hewlett Packard Enterprise
[Test Sponsor: HPE]
Synergy 480 Gen10 Plus
(3.00 GHz, Intel Xeon Gold 5317)

SPECrate®2017_fp_base = 228
SPECrate®2017_fp_peak = 234

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Synergy 480 Gen10 Plus
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Test Sponsor: HPE
Tested by: HPE

Test Date: Dec-2021
Hardware Availability: Nov-2021
Software Availability: Dec-2020

Base Optimization Flags (Continued)

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-stdlib=lib64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-stdlib=lib64-5.0.1/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -stdlib=lib64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-stdlib=lib64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -stdlib=lib64-5.0.1/lib

Peak Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

(Continued on next page)
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Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
511.povray_r: icpc icc
526.blender_r: icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-Ofast -qopt-mem-layout-trans=4
-fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
508.namd_r: basepeak = yes
510.parest_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

(Continued on next page)
Hewlett Packard Enterprise  
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Peak Optimization Flags (Continued)

Fortran benchmarks:

503.bwaves_r.basepeak = yes
549.fotonik3d_r.basepeak = yes
554.roms_r -w -m64 -W1,-z,muldefs -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:

521.wrf_r.basepeak = yes
527.cam4_r.basepeak = yes

Benchmarks using both C and C++:

511.povray_r -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

526.blender_r.basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r.basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revG.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revG.xml
### SPEC CPU®2017 Floating Point Rate Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
Synergy 480 Gen10 Plus  
(3.00 GHz, Intel Xeon Gold 5317)

<table>
<thead>
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**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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