Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10 Plus
(2.40 GHz, Intel Xeon Silver 4314)

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Hardware
CPU Name: Intel Xeon Silver 4314
Max MHz: 3400
Nominal: 2400
Enabled: 32 cores, 2 chips
Orderable: 1, 2 chip(s)
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 24 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)
Storage: 1 x 800 GB SAS SSD, RAID 0
Other: None

Software
OS: Red Hat Enterprise Linux 8.3 (Ootpa)
Kernel 4.18.0-240.el8.x86_64
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler
Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler
Classic Build 20201112 for Linux
Parallel: Yes
Firmware: HPE BIOS Version I44 v1.54 11/03/2021 released Nov-2021
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>32</td>
<td>254</td>
<td>6.98</td>
<td>254</td>
<td>6.99</td>
<td>256</td>
<td>6.95</td>
<td>32</td>
<td>220</td>
<td>8.06</td>
<td>222</td>
<td>8.00</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>32</td>
<td>387</td>
<td>10.3</td>
<td>385</td>
<td>10.3</td>
<td>388</td>
<td>10.2</td>
<td>32</td>
<td>375</td>
<td>10.6</td>
<td>376</td>
<td>10.6</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>32</td>
<td>250</td>
<td>18.9</td>
<td>249</td>
<td>18.9</td>
<td>249</td>
<td>19.0</td>
<td>32</td>
<td>250</td>
<td>18.9</td>
<td>249</td>
<td>18.9</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>32</td>
<td>114</td>
<td>12.5</td>
<td>112</td>
<td>12.7</td>
<td>109</td>
<td>13.0</td>
<td>32</td>
<td>114</td>
<td>12.5</td>
<td>112</td>
<td>12.7</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>32</td>
<td>249</td>
<td>5.75</td>
<td>249</td>
<td>5.75</td>
<td>250</td>
<td>5.74</td>
<td>32</td>
<td>249</td>
<td>5.75</td>
<td>250</td>
<td>5.74</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>32</td>
<td>363</td>
<td>4.71</td>
<td>362</td>
<td>4.71</td>
<td>363</td>
<td>4.70</td>
<td>32</td>
<td>363</td>
<td>4.71</td>
<td>362</td>
<td>4.71</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>32</td>
<td>157</td>
<td>18.8</td>
<td>156</td>
<td>18.8</td>
<td>156</td>
<td>18.8</td>
<td>32</td>
<td>157</td>
<td>18.8</td>
<td>156</td>
<td>18.8</td>
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</table>

**SPECspeed**®2017_int_base = 11.2
**SPECspeed**®2017_int_peak = 11.4

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

- Stack size set to unlimited using "ulimit -s unlimited"
- Transparent Huge Pages enabled by default
- Prior to runcpu invocation
- Filesystem page cache synced and cleared with:
  ```
  sync; echo 3 > /proc/sys/vm/drop_caches
  ```

## Environment Variables Notes

- Environment variables set by runcpu before the start of the run:
  ```
  KMP_AFFINITY = "granularity=fine,scatter"
  LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
  MALLOC_CONF = "retain:true"
  OMP_STACKSIZE = "192M"
  ```

## General Notes

- Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
- NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
- Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
- Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
- jemalloc, a general purpose malloc implementation
- built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
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General Notes (Continued)


Submitted by: "Bucek, James" <jemalloc@hpe.com>
Submitted: Wed Jan 12 10:02:54 EST 2022
Submission: cpu2017-20220103-30726.sub

Platform Notes

BIOS Configuration:
Workload Profile set to General Peak Frequency Compute
Intel Hyper-Threading set to Disabled
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
Advanced Memory Protection set to Advanced ECC
Last Level Cache (LLC) Prefetch set to Enabled
Last Level Cache (LLC) Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Power
DCU Stream Prefetcher set to Disabled
Adjacent Sector Prefetch set to Disabled
Minimum Processor Idle Power Package C-State set to No Package State
Numa Group Size Optimization set to Flat

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca6c64d
running on localhost.localdomain Tue Dec 14 19:24:37 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu from util-linux 2.32.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit

(Continued on next page)
Platform Notes (Continued)

Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
Stepping: 6
CPU MHz: 1742.535
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 24576K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrnr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
mib ibpb stibp ibrs_enhanced tpr_shadow vmni flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm rdtdq_cqfd sha_ha avx512bw
avx512vl xsaveopt xsaves xsaveopt xstate cqm l1c qmmi l1d qnseq_coll l1d qpseq_coll
l1d qm bmem local split_lock_detect wboinevd dtherm ida arat pin pts avx512vnni umip pku
ospke avx512_vbmi2 gfnv vaes vplcmulqdq avx512_vnni avx512_bitalg tme
avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

/cache data
cache size: 24576 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 1006789 MB
node 0 free: 1030990 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 1006524 MB
node 1 free: 1031522 MB

(Continued on next page)
### SPEC CPU®2017 Integer Speed Result

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<table>
<thead>
<tr>
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<tr>
<td>CPU2017 License: 3</td>
<td>Test Date: Dec-2021</td>
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<td>Hardware Availability: Nov-2021</td>
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<td>Software Availability: Dec-2020</td>
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</tbody>
</table>

#### Platform Notes (Continued)

- **node distances:**
  - node 0 1
  - 0: 10 20
  - 1: 20 10

- From /proc/meminfo
  - MemTotal: 2113495316 kB
  - HugePages_Total: 0
  - Hugepagesize: 2048 kB

- /sbin/tuned-adm active
  - Current active profile: throughput-performance

- From /etc/*release* /etc/*version*
  - os-release:
    - NAME="Red Hat Enterprise Linux"
    - VERSION="8.3 (Ootpa)"
    - ID="rhel"
    - ID_LIKE="fedora"
    - VERSION_ID="8.3"
    - PLATFORM_ID="platform:el8"
    - PRETTY_NAME="Red Hat Enterprise Linux 8.3 (Ootpa)"
    - ANSI_COLOR="0;31"
  - redhat-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
  - system-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
  - system-release-cpe: cpe:/o:redhat:enterprise_linux:8.3:ga

- uname -a:
  - Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Wed Sep 23 05:13:10 EDT 2020
  - x86_64 x86_64 x86_64 GNU/Linux

#### Kernel self-reported vulnerability status:

- **CVE-2018-12207 (iTLB Multihit):** Not affected
- **CVE-2018-3620 (L1 Terminal Fault):** Not affected
- **Microarchitectural Data Sampling:** Not affected
- **CVE-2017-5754 (Meltdown):** Not affected
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: usercopy/swaps barriers and __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- **CVE-2020-0543 (Special Register Buffer Data Sampling):** Not affected
- **CVE-2019-11135 (TSX Asynchronous Abort):** Not affected

(Continued on next page)
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Platform Notes (Continued)

run-level 3 Dec 14 19:23
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs 670G 111G 559G 17% /home
From /sys/devices/virtual/dmi/id
Vendor: HPE
Product: Synergy 480 Gen10 Plus
Product Family: Synergy
Serial: CN70330Q5F

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x Micron 36ASF8G72PZ-3G2B2 64 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: HPE
BIOS Version: I44
BIOS Date: 11/03/2021
BIOS Revision: 1.54
Firmware Revision: 2.40

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>600.perlbench_s(peak)</th>
</tr>
</thead>
</table>
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
| 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak) |
| 625.x264_s(base, peak) 657.xz_s(base, peak) |
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

(Continued on next page)
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Hardware Availability: Nov-2021
Software Availability: Dec-2020

Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort
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---

**Base Portability Flags**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench</td>
<td>-DSPEC_LP64 -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>gcc</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>mcf</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>omnetpp</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>xalancbmk</td>
<td>-DSPEC_LP64 -DSPEC_LINUX</td>
</tr>
<tr>
<td>x264</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>deepsjeng</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>leela</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>exchange2</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>xz</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

---

**Base Optimization Flags**

**C benchmarks:**
-DSPEC_OPENMP -std=c11 -m64 -fopenmp -Wl,-z,muldefs -xCORE-AVX512  
-03 -ffast-math -flto -mfpmath=sse -funroll-loops  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc  

**C++ benchmarks:**
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math  
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4  
-mbranches-within-32B-boundaries  
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/  
-1qkmalloc  

**Fortran benchmarks:**
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4  
-nostandard-realloc-lhs -align array32byte -auto  
-mbranches-within-32B-boundaries

---

**Peak Compiler Invocation**

**C benchmarks (except as noted below):**  
`icx`  

600.perlbench_s: `icc`  

**C++ benchmarks:**  
`icpx`

(Continued on next page)
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Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

602.gcc_s: -m64 -std=c11 -Wl, -z, muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

605.mcf_s: basepeak = yes

625.x264_s: -DSPEC_OPENMP -fiopenmp -std=c11 -m64 -Wl, -z, muldefs
-xCORE-AVX512 -flto -O3 -ffast-math
-qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

657.xz_s: basepeak = yes

C++ benchmarks:

620.omnetpp_s: basepeak = yes

623.xalancbmk_s: basepeak = yes

631.deepsjeng_s: basepeak = yes

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Peak Optimization Flags (Continued)

641.leela_s: basepeak = yes

Fortran benchmarks:

648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at:
[http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revG.html](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revG.html)

You can also download the XML flags sources by saving the following links:
[http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revG.xml](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revG.xml)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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