SPEC CPU®2017 Floating Point Rate Result

Dell Inc.
PowerEdge C6420 (Intel Xeon Silver 4215R, 3.20 GHz)

SPECrated®2017_fp_base = 115
SPECrated®2017_fp_peak = 119

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Nov-2021
Hardware Availability: Feb-2020
Software Availability: May-2021

Copies
503.bwaves_r 32
16

507.caCTuBSSN_r 32

508.namd_r 32
72.4

510.parest_r 32
60.2

511.povray_r 32
137

519.lbm_r 32
62.2

521.wrf_r 32
121

526.blender_r 32
116

527.cam4_r 32
98.6

538.imagick_r 32

544.nab_r 32
165

549.fotonik3d_r 32
101

554.roms_r 32
50.6

--- SPECrated®2017_fp_base (115) ---

--- SPECrated®2017_fp_peak (119) ---

Hardware

CPU Name: Intel Xeon Silver 4215R
Max MHz: 4000
Nominal: 3200
Enabled: 16 cores, 2 chips, 2 threads/core
Orderable: 1,2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 11 MB I+D on chip per core
Other: None
Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)
Storage: 1 x 1.6 TB SATA SSD
Other: None

Software

OS: Red Hat Enterprise Linux 8.4 (Ootpa)
        4.18.0-305.el8.x86_64
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
        Compiler Build 20201113 for Linux;
        Fortran: Version 2021.1 of Intel Fortran Compiler
        Classic Build 20201112 for Linux;
        C/C++: Version 2021.1 of Intel C/C++ Compiler
        Classic Build 20201112 for Linux
Parallel: No
Firmware: Version 2.11.2 released Apr-2021
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance
        at the cost of additional power usage.
## SPEC CPU®2017 Floating Point Rate Result

### Dell Inc.

**PowerEdge C6420 (Intel Xeon Silver 4215R, 3.20 GHz)**

**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
**Tested by:** Dell Inc.  

**SPECrater®2017_fp_base = 115**

**SPECrater®2017_fp_peak = 119**

**Test Date:** Nov-2021  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2021

### Results Table

<table>
<thead>
<tr>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
<td>503.bwaves_r</td>
<td>32</td>
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<td>302</td>
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<td>16</td>
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<td>507.cactuBSSN_r</td>
<td>32</td>
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<td>420</td>
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<td>632</td>
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<td>521.wrf_r</td>
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<tr>
<td>526.blender_r</td>
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<tr>
<td>538.imagick_r</td>
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<td></td>
</tr>
<tr>
<td>544.nab_r</td>
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<td>326</td>
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<td>32</td>
<td>325</td>
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<td>549.fotonik3d_r</td>
<td>32</td>
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<td>1217</td>
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<td>32</td>
<td>1234</td>
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<td>1217</td>
<td>102</td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>32</td>
<td>1003</td>
<td>50.7</td>
<td>1004</td>
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<td>16</td>
<td>418</td>
<td>60.8</td>
<td>418</td>
<td>60.9</td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
    "/root/cpu2017-1.1.8-ic2021.1/lib/intel64:/root/cpu2017-1.1.8-ic2021.1/j
e5.0.1-64"
MALLOCONF = "retain:true"
```

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Red Hat Enterprise Linux 8.1. Transparent Huge Pages enabled by default.

(Continued on next page)
Dell Inc.
PowerEdge C6420 (Intel Xeon Silver 4215R, 3.20 GHz)

SPECrate®2017_fp_base = 115
SPECrate®2017_fp_peak = 119

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Nov-2021
Hardware Availability: Feb-2020
Software Availability: May-2021

General Notes (Continued)

Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numaclt i.e.:
numactl --interleave=all runcpu <etc>
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

Platform Notes

BIOS settings:
Sub NUMA Cluster : 2-Way Clustering
Virtualization Technology : Disabled

System Profile : Custom
CPU Power Management : Maximum Performance
C1E : Disabled
C States : Autonomous
Memory Patrol Scrub : Disabled
Energy Efficiency Policy : Performance
CPU Interconnect Bus Link
Power Management : Disabled
PCI ASPM L1 Link
Power Management : Disabled

Sysinfo program /root/cpu2017-1.1.8-ic2021.1/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on localhost.localdomain Sun Nov 28 15:03:48 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
2 "physical id"s (chips)
32 "processors"
**Dell Inc.**

**PowerEdge C6420 (Intel Xeon Silver 4215R, 3.20 GHz)**

**SPEC CPU®2017 Floating Point Rate Result**

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
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**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
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---

**Platform Notes (Continued)**

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

```plaintext
cpu cores : 8
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7
```

From lscpu from util-linux 2.32.1:

- **Architecture:** x86_64
- **CPU op-mode(s):** 32-bit, 64-bit
- **Byte Order:** Little Endian
- **CPU(s):** 32
- **On-line CPU(s) list:** 0-31
- **Thread(s) per core:** 2
- **Core(s) per socket:** 8
- **Socket(s):** 2
- **NUMA node(s):** 2
- **Vendor ID:** GenuineIntel
- **BIOS Vendor ID:** Intel
- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
- **BIOS Model name:** Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
- **Stepping:** 7
- **CPU MHz:** 3599.990
- **CPU max MHz:** 4000.0000
- **CPU min MHz:** 1000.0000
- **BogoMIPS:** 6400.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 11264K
- **NUMA node0 CPU(s):** 0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30
- **NUMA node1 CPU(s):** 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrmm pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_patin ssbd mba ibrs ibpb stibp ibrs_enhanced fsbgbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cmq mxp rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xaxvec xgetbv1 xsaveas cmq_llc cmq_occupy_llc cmq_mmb_total cmq_mmb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d arch_capabilities

(Continued on next page)
Dell Inc.
PowerEdge C6420 (Intel Xeon Silver 4215R, 3.20 GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2022 Standard Performance Evaluation Corporation

SPECrate®2017_fp_base = 115
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CPU2017 License: 55
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Software Availability: May-2021

Platform Notes (Continued)

/proc/cpuinfo cache data
  cache size : 11264 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30
  node 0 size: 192074 MB
  node 0 free: 180786 MB
  node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31
  node 1 size: 193494 MB
  node 1 free: 178144 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 394822444 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/sbin/tuned-adm active
  Current active profile: throughput-performance
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
  os-release:
    NAME="Red Hat Enterprise Linux"
    VERSION="8.4 (Ootpa)"
    ID="rhel"
    ID_LIKE="fedora"
    VERSION_ID="8.4"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="Red Hat Enterprise Linux 8.4 (Ootpa)"
    ANSI_COLOR="0;31"
  redhat-release: Red Hat Enterprise Linux release 8.4 (Ootpa)
  system-release: Red Hat Enterprise Linux release 8.4 (Ootpa)
  system-release-cpe: cpe:/o:redhat:enterprise_linux:8.4:ga

uname -a:
  Linux localhost.localdomain 4.18.0-305.el8.x86_64 #1 SMP Thu Apr 29 08:54:30 EDT 2021
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

(Continued on next page)
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Platform Notes (Continued)

CVE-2018-12207 (iTLB Multi-hit): KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store
CVE-2018-3639 (Speculative Store Bypass): Bypass disabled via prctl and
CVE-2017-5753 (Spectre variant 1): seccomp
CVE-2017-5715 (Spectre variant 2): Mitigation: usercopy/swaps
cve-2017-5753 (Meltdown): barriers and __user pointer
CVE-2020-0543 (Special Register Buffer Data Sampling): Mitigation: Speculative Store
CVE-2019-11135 (TSX Asynchronous Abort): Bypass disabled via prctl and
run-level 3 Nov 28 09:48
Mitigation: Speculative Store

KVM: Mitigation: Split huge pages
Not affected
Not affected
Mitigation: Speculative Store
Bypass disabled via prctl and
seccomp
Mitigation: usercopy/swaps
cbarriers and __user pointer
Mitigation: Enhanced IBRS, IBPB:
sanitization
conditional, RSB filling
Mitigation: TSX disabled

run-level 3 Nov 28 09:48

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda2      xfs   693G   37G  656G   6% /

From /sys/devices/virtual/dmi/id
Vendor: Dell Inc.
Product: PowerEdge C6420
Product Family: PowerEdge

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
1x 002C069D002C 36ASF4G72PZ-2G9E2 32 GB 2 rank 2933, configured at 2400
4x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933, configured at 2400
6x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933, configured at 2400
1x 00AD069D00AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933, configured at 2400

BIOS:
BIOS Vendor: Dell Inc.
BIOS Version: 2.11.2
BIOS Date: 04/22/2021
BIOS Revision: 2.11

(End of data from sysinfo program)
Compiler Version Notes

C

| 519.lbm_r(base, peak) 538.imagick_r(base, peak) |
| 544.nab_r(base, peak) |

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++

| 508.namd_r(base, peak) 510.parest_r(base, peak) |

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C

| 511.povray_r(peak) |

Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C

| 511.povray_r(base) 526.blender_r(base, peak) |

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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C++, C

| 511.povray_r(peak) |

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(Continued on next page)
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Compiler Version Notes (Continued)

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==============================================================================
C++, C          | 511.povray\_r(base) 526.blender\_r(base, peak)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
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==============================================================================
C++, C, Fortran | 507.cactuBSSN\_r(base, peak)
==============================================================================
Fortran         | 503.bwaves\_r(base, peak) 549.fotonik3d\_r(base, peak)
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C      | 521.wrf\_r(base, peak) 527.cam4\_r(base, peak)
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
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SPEC CPU®2017 Floating Point Rate Result

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---

**Base Compiler Invocation**

C benchmarks:
- icx

C++ benchmarks:
- icpx

Fortran benchmarks:
- ifort

Benchmarks using both Fortran and C:
- ifort icx

Benchmarks using both C and C++:
- icpx icx

Benchmarks using Fortran, C, and C++:
- icpx icx ifort

---

**Base Portability Flags**

503.bwaves_r: -DSPEC_LP64
507.cactusBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

---

**Base Optimization Flags**

C benchmarks:
- -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
- -ftol -mfpmath=sse -funroll-loops -gopt-mem-layout-trans=4
- -mbranches-within-32B-boundaries -ljemalloc
- -L/usr/local/jemalloc64-5.0.1/lib

(Continued on next page)
Dell Inc.  
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Base Optimization Flags (Continued)

C++ benchmarks:
-\text{-w} -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math -flto
-\text{-mfpmath}=sse \text{-funroll-loops} \text{-qopt-mem-layout-trans}=4
-\text{-mbranches-within-32B-boundaries}\text{-ljemalloc}
-\text{-L/usr/local/jemalloc64-5.0.1/lib}

Fortran benchmarks:
-\text{-w} -m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 \text{-ipo} \text{-no-prec-div}
-\text{-qopt-prefetch} \text{-ffinite-math-only}
-\text{-qopt-multiple-gather-scatter-by-shuffles} \text{-qopt-mem-layout-trans}=4
-\text{-nostandard-realloc-lhs}\text{-align array32byte}\text{-auto}
-\text{-mbranches-within-32B-boundaries}\text{-ljemalloc}
-\text{-L/usr/local/jemalloc64-5.0.1/lib}

Benchmarks using both Fortran and C:
-\text{-w} -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-\text{-flto} \text{-mfpmath}=sse \text{-funroll-loops} \text{-qopt-mem-layout-trans}=4 \text{-O3}\text{-ipo}
-\text{-no-prec-div}\text{-qopt-prefetch}\text{-ffinite-math-only}
-\text{-qopt-multiple-gather-scatter-by-shuffles}
-\text{-mbranches-within-32B-boundaries}\text{-nostandard-realloc-lhs}
-\text{-align array32byte}\text{-auto}\text{-ljemalloc}\text{-L/usr/local/jemalloc64-5.0.1/lib}

Benchmarks using both C and C++:
-\text{-w} -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-\text{-flto} \text{-mfpmath}=sse \text{-funroll-loops} \text{-qopt-mem-layout-trans}=4
-\text{-mbranches-within-32B-boundaries}\text{-ljemalloc}
-\text{-L/usr/local/jemalloc64-5.0.1/lib}

Benchmarks using Fortran, C, and C++:
-\text{-w} -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-\text{-flto} \text{-mfpmath}=sse \text{-funroll-loops} \text{-qopt-mem-layout-trans}=4 \text{-O3}
-\text{-no-prec-div}\text{-qopt-prefetch}\text{-ffinite-math-only}
-\text{-qopt-multiple-gather-scatter-by-shuffles}
-\text{-mbranches-within-32B-boundaries}\text{-nostandard-realloc-lhs}
-\text{-align array32byte}\text{-auto}\text{-ljemalloc}\text{-L/usr/local/jemalloc64-5.0.1/lib}

Peak Compiler Invocation

C benchmarks: \text{icx}

C++ benchmarks: \text{icpx}
Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
511.povray_r: icpx icc
526.blender_r: icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX2 -ftto
-Ofast -gopt-mem-layout-trans=4
-fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
508.namd_r: basepeak = yes
510.parest_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-ftto -mfpmath=sse -funroll-loops
-gopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

(Continued on next page)
Peak Optimization Flags (Continued)

Fortran benchmarks:

503.bwaves_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ipo
-no-prec-div -gopt-prefetch -ffinite-math-only
-gopt-multiple-gather-scatter-by-shuffles
-gopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: basepeak = yes

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2 -O3 -ipo
-no-prec-div -gopt-prefetch -ffinite-math-only
-gopt-multiple-gather-scatter-by-shuffles
-gopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-Intel-ICX-rev1.5.xml
# SPEC CPU®2017 Floating Point Rate Result

## Dell Inc.

**PowerEdge C6420 (Intel Xeon Silver 4215R, 3.20 GHz)**

<table>
<thead>
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<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
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<tr>
<td>115</td>
<td>119</td>
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</tbody>
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**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
**Tested by:** Dell Inc.  
**Test Date:** Nov-2021  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2021

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-11-28 15:03:47-0500.  
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