Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7513)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base =</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak =</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2022
Hardware Availability: Aug-2021
Software Availability: Dec-2021

C has determined that this result does not comply with the SPEC CPU 2017 run and reporting rules. Specifically, the submitter notified SPEC that the system as configured violates rule 2.3.1 (a) due to the use of an unsafe compiler option.

<table>
<thead>
<tr>
<th>Copies</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
</tr>
<tr>
<td>502.gcc_r</td>
</tr>
<tr>
<td>505.mcf_r</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
</tr>
<tr>
<td>525.x264_r</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
</tr>
<tr>
<td>541.leela_r</td>
</tr>
<tr>
<td>548.exchange2_r</td>
</tr>
<tr>
<td>557.xz_r</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: AMD EPYC 7513</td>
</tr>
<tr>
<td>Nominal: 2600</td>
</tr>
<tr>
<td>Enabled: 64 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable: 1.2 chips</td>
</tr>
<tr>
<td>Cache L1: 22 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2: 512 KB I+D on chip per core</td>
</tr>
<tr>
<td>L3: 128 MB I+D on chip per chip, 32 MB shared / 8 cores</td>
</tr>
<tr>
<td>Other: None</td>
</tr>
<tr>
<td>Memory: 2 TB (16 x 128 GB 4Rx4 PC4-3200V-L)</td>
</tr>
<tr>
<td>Storage: 1 x 960 GB M.2 SSD SATA</td>
</tr>
<tr>
<td>Other: None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 SP3 (x86_64) kernel version 5.3.18-57-default</td>
</tr>
<tr>
<td>Compiler: C/C++/Fortran: Version 3.0.0 of AOCC</td>
</tr>
<tr>
<td>Parallel: No</td>
</tr>
<tr>
<td>Firmware: Version 4.2.1 released Feb-2022</td>
</tr>
<tr>
<td>File System: xfs</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>Peak Pointers: 32/64-bit</td>
</tr>
<tr>
<td>Other: jemalloc: jemalloc memory allocator library v5.1.0</td>
</tr>
<tr>
<td>Power Management: BIOS and OS set to prefer performance at the cost of additional power usage</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7513)

SPECrate®2017_int_base =
SPECrate®2017_int_peak =

Results Table

<table>
<thead>
<tr>
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<th>Seconds</th>
<th>Ratio</th>
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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The AMD64 AOCC Compiler Suite is available at http://developer.amd.com/amd-aocc/

Submit Notes

The config file option 'submit' was used.
'numactl' was used to bind copies to the cores.
See the configuration file for details.

Operating System Notes

'ulimit -s unlimited' was used to set environment stack size limit
'ulimit -l 2097152' was used to set environment locked pages in memory limit

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7513)

SPECrate®2017_int_base = SPECrate®2017_int_peak =

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2022
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Operating System Notes (Continued)

To limit dirty cache to 8% of memory, 'sysctl -w vm.dirty_ratio=8' run as root.
To limit swap usage to minimum necessary, 'sysctl -w vm.swappiness=1' run as root.
To free node-local memory and avoid remote memory usage,
'local -w vm.zone_reclaim_mode=1' run as root.
To clear filesystem caches, 'sync; sysctl -w vm.drop_caches=3' run as root.
To disable address space layout randomization (ASLR) to reduce run-to-run
variability, 'sysctl -w kernel.randomize_va_space=0' run as root.

To enable Transparent Hugepages (THP) on request for base runs,
'echo madvise > /sys/kernel/mm/transparent_hugepage/enabled' run as root.
To enable THP for all allocations for peak runs,
'echo always > /sys/kernel/mm/transparent_hugepage/enabled' and
'echo always > /sys/kernel/mm/transparent_hugepage/defrag' run as root.

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/amd_rate_aocc300_milan_B_lib/lib;/home/cpu2017/amd_rate_aocc300_milan_B_lib32:" MALLOC_CONF = "retain:true"

Environment variables set by runcpu during the 523.xalancbmk_r peak run:
MALLOC_CONF = "thp:never" 

General Notes

Binaries were compiled on a system with 2x AMD EPYC 7742 CPU + 1TiB Memory using OpenSUSE 15.2

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc: configured and built with GCC v4.8.2 in RHEL 7.4 (No options specified)

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7513)

SPECrating®2017_int_base =
SPECrating®2017_int_peak =

CPU2017 License: 9019
Test Date: Jul-2022
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CPU2017 License: 9019
Test Date: Jul-2022
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Copyright 2017-2023 Standard Performance Evaluation Corporation

SPEC has determined that this result does not comply with the SPEC CPU 2017 run and reporting rules. Specifically, the submitter notified SPEC that the system as configured violates rule 2.3.1 (a) due to the use of an unsafe compiler option.

General Notes (Continued)
jemalloc 5.1.0 is available here:
https://github.com/jemalloc/jemalloc/releases/download/5.1.0/jemalloc-5.1.0.tar.bz2

Platform Notes

BIOS Configuration
SMT Mode set to Enabled
NUMA nodes per socket set to NPS4
ACPI SRAT L3 Cache As NUMA Domain set to Enabled
DRAM Scrub Time set to Disabled
Determinism Slider set to Power
Memory Interleaving set to Disabledd
APBDIS set to 1

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on SPEC-SRV Thu Jul 28 06:21:18 2022

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : AMD EPYC 7513 32-Core Processor
physical id"s (chips)
 cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cores : 32
siblings : 64

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

From lscpu from util-linux 2.36.2:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit

(Continued on next page)
Non-Compliant

SPEC has determined that this result does not comply with the SPEC CPU 2017 run and reporting rules. Specifically, the submitter notified SPEC that the system as configured violates rule 2.3.1 (a) due to the use of an unsafe compiler option.
**SPEC CPU®2017 Integer Rate Result**

**Cisco Systems**

Cisco UCS C225 M6 (AMD EPYC 7513)

| SPECrate®2017_int_base = |
| SPECrate®2017_int_peak = |

**CPU2017 License:** 9019
**Test Sponsor:** Cisco Systems
**Tested by:** Cisco Systems
**Test Date:** Jul-2022
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**Software Availability:** Dec-2021

---

**Platform Notes (Continued)**

IBRS_FW, STIBP always-on, RSB filling
Vulnerability Srbds: Not affected
Vulnerability Tsx async abort: Not affected
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr
       pge mca cmov pat pse36 clflush mlxi extmsrl xsaveopt xsaves xsavecntr xsave
       clflushopt clwb contentsismt lbmr svm_lock

From lscpu --cache:

<table>
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<tr>
<th>NAME</th>
<th>ONE-SIZE</th>
<th>ALL-SIZE</th>
<th>WAYS</th>
<th>TYPE</th>
<th>LEVEL</th>
<th>SETS</th>
<th>PHYS-LINE</th>
<th>COHERENCY-SIZE</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1d</td>
<td>32K</td>
<td>2M</td>
<td>8</td>
<td>Data</td>
<td>1</td>
<td>64</td>
<td>1</td>
<td>64</td>
</tr>
<tr>
<td>L1i</td>
<td>32K</td>
<td>2M</td>
<td>8</td>
<td>Instruction</td>
<td>1</td>
<td>64</td>
<td>1</td>
<td>64</td>
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<tr>
<td>L2</td>
<td>32M</td>
<td>32M</td>
<td>8</td>
<td>Unified</td>
<td>2</td>
<td>1024</td>
<td>1</td>
<td>64</td>
</tr>
<tr>
<td>L3</td>
<td>32M</td>
<td>256M</td>
<td>16</td>
<td>Unified</td>
<td>3</td>
<td>32768</td>
<td>1</td>
<td>64</td>
</tr>
</tbody>
</table>

From numactl --hardware

**WARNING:** a numactl 'node' might or might not correspond to a physical chip.

available: 8 nodes (0-7)
node 0 cpus: 0 1 2 3 4 5 6 7 64 65 66 67 68 69 70 71
node 0 size: 257785 MB
node 0 free: 257472 MB
node 1 cpus: 8 9 10 11 12 13 14 15 72 73 74 75 76 77 78 79
node 1 size: 258042 MB
node 1 free: 257700 MB
node 2 cpus: 16 17 18 19 20 21 22 23 80 81 82 83 84 85 86 87
node 2 size: 258042 MB
node 2 free: 257641 MB
node 3 cpus: 24 25 26 27 28 29 30 31 88 89 90 91 92 93 94 95
node 3 size: 257700 MB
node 3 free: 257472 MB
node 4 cpus: 4 5 6 7 40 41 42 43 44 45 46 47 48 49 50 51 52 53
node 4 size: 257785 MB
node 4 free: 257472 MB
node 5 cpus: 8 9 10 11 12 13 14 15 54 55 56 57 58 59 60 61
node 5 size: 258042 MB
node 5 free: 257700 MB
node 6 cpus: 16 17 18 19 20 21 22 23 62 63 64 65 66 67 68 69
node 6 size: 258042 MB
node 6 free: 257641 MB
node 7 cpus: 24 25 26 27 28 29 30 31 70 71 72 73 74 75 76 77
node 7 size: 257785 MB
node 7 free: 257472 MB

---

**Non-Compliant**

SPEC has determined that this result does not comply with the SPEC CPU 2017 run and reporting rules. Specifically, the submitter notified SPEC that the system as configured violates rule 2.3.1 (a) due to the use of an unsafe compiler option.
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7513)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
CPU2017 Rate: SPECrate®2017_int_peak =
               SPECrate®2017_int_base =

C has determined that this result does not comply with the SPEC CPU 2017 run and reporting rules. Specifically, the submitter notified SPEC that the system as configured violates rule 2.3.1 (a) due to the use of an unsafe compiler option.

Platform Notes (Continued)

node 3 size: 258030 MB
node 3 free: 257742 MB
node 4 cpus: 32 33 34 35 36 37 38 39 96 101 102 103
node 4 size: 258042 MB
node 4 free: 257744 MB
node 5 cpus: 40 41 42 43 44 45 46 47 105 106 107 108 109 110 111
node 5 size: 258042 MB
node 5 free: 257783 MB
node 6 cpus: 48 49 50 51 52 53 54 55 112 113 114 115 116 117 118 119
node 6 size: 258042 MB
node 6 free: 257731 MB
node 7 cpus: 56 57 58 59 60 61 62 63 120 121 122 123 124 125 126 127
node 7 size: 257763 MB
node 7 free: 257505 MB
node distances:
node 0 1 2 3 5 6 7
  0: 10 12 12 12 32 32 32
  1: 12 10 11 12 32 32 32
  2: 12 12 12 12 32 32 32
  3: 12 12 12 10 32 32 32
  4: 32 32 32 10 32 32 32
  5: 32 32 32 32 32 32 32
  6: 32 32 32 32 32 32 32
  7: 32 32 32 32 32 32 32

From /proc/meminfo
MemTotal:       2113324672 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

(sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP3"
VERSION_ID="15.3"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
ID="sles"

(Continued on next page)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7513) SPECrate®2017_int_base = SPECrate®2017_int_peak =

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Platform Notes (Continued)

ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp3"

uname -a:
Linux SPEC-SRV 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Full AMD retpoline, IBFB: conditional, IBRS_FW, STIBF: always-on, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Apr 29 12:00
 SPEC is set to: /home/cpu2017
 Filesystem Type Size Used Avail Use% Mounted on
 /dev/sdb4 xfs 180G 21G 160G 12% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCS-C225-M6S
Serial: WZP2524931G

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are
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CPU2017 License: 9019  Test Date: Jul-2022
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Platform Notes (Continued)

frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
16x 0xCE00 M386AAG40AM3-CWE 128 GB 4 rank 32
BIOS:
  BIOS Vendor: Cisco Systems, Inc.
  BIOS Version: C225M6.4.2.1.28.0217220401
  BIOS Date: 02/17/2022
  BIOS Revision: 5.21

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
------------------------------------------------------------------------------

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
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Software Availability: Dec-2021

---

Compiler Version Notes (Continued)

LLVM Mirror.Version.12.0.0
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

C++

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

C++

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

C++

Non-Compliant

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Compiler Version Notes (Continued)

-----------------------------------------------
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
-----------------------------------------------

C++
---
520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

-----------------------------------------------
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
-----------------------------------------------

Fortran
---
548.exchange2_r(base, peak)

-----------------------------------------------
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
-----------------------------------------------

Base Compiler Invocation

C benchmarks:
clang

C++ benchmarks:
clang++

Fortran benchmarks:
flang

------------------------------------------------------------------------------
Non-Compliant
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and reporting rules. Specifically, the submitter notified SPEC that the system as
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2022
Hardware Availability: Aug-2021
Software Availability: Dec-2021

Non-Compliant

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**Base Portability Flags**

- 500.perlbench_r: -DSPEC_LINUX_X64 -DSPEC_LP64
- 502.gcc_r: -DSPEC_LP64
- 505.mcf_r: -DSPEC_LP64
- 520.omnetpp_r: -DSPEC_LP64
- 523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
- 525.x264_r: -DSPEC_LP64
- 531.deepsjeng_r: -DSPEC_LP64
- 541.leela_r: -DSPEC_LP64
- 548.exchange2_r: -DSPEC_LP64
- 557.xz_r: -DSPEC_LP64

**Base Optimization Flags**

**C benchmarks:**
- -m64 -Wl,-allow-multiple-definition -Wl,-mlllvm -Wl,-enable-licm-vrp
- -flto -Wl,-mlllvm -Wl,-region-vectorize
- -Wl,-mlllvm -Wl,-function-specialize
- -Wl,-mlllvm -Wl,-align-all-nofallthru-blocks=6
- -Wl,-mlllvm -Wl,-reduce-array-computations=3 -O3 -ffast-math
- -march=znver3 -fveclib=AMDLIBM -fstruct-layout=5
- -mllvm -unroll-threshold=50 -mlllvm -inline-threshold=1000
- -fremap-arrays -mlllvm -function-specialize -flv-function-specialization
- -mlllvm -enable-gvn-hoist -mlllvm -global-vectorize-slp=true
- -flto -mlllvm -licm-vrp -mlllvm -reduce-array-computations=3 -z muldefs
- -lamdlibm -ljemalloc -lflang -lflangrti

**C++ benchmarks:**
- -m64 -std=c++98 -Wl,-mlllvm -Wl,-do-block-reorder=aggressive -flto
- -Wl,-mlllvm -Wl,-region-vectorize -Wl,-mlllvm -Wl,-function-specialize
- -Wl,-mlllvm -Wl,-align-all-nofallthru-blocks=6
- -Wl,-mlllvm -Wl,-reduce-array-computations=3 -O3 -ffast-math
- -march=znver3 -fveclib=AMDLIBM -mlllvm -enable-partial-unswitch
- -mlllvm -unroll-threshold=100 -finline-aggressive
- -flv-function-specialization -mlllvm -loop-unswitch=threshold=200000
- -mlllvm -reroll-loops -mlllvm -aggressive-loop-unswitch
- -mlllvm -extra-vectorizer-passes -mlllvm -reduce-array-computations=3
- -mlllvm -global-vectorize-slp=true -mlllvm -convert-pow-exp-to-int=false

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Base Optimization Flags (Continued)

C++ benchmarks (continued):
-z muldefs -mlllvm -do-block-reorder=aggressive
-fvirtual-function-elimination -fvisibility=hidden -lamdlibm
-ljemalloc -lflang -lflangrti

Fortran benchmarks:
-m64 -Wl,-mlllvm -Wl,-inline-recursion=4
-Wl,-mlllvm -Wl,-lsr-in-nested-loop -Wl,-mlllvm -Wl,-enable-iv-split
-flto -Wl,-mlllvm -Wl,-region-vectorize
-Wl,-mlllvm -Wl,-function-specialize
-Wl,-mlllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mlllvm -Wl,-reduce-array-computations=3 -O3 -ffast-math
-march=znver3 -fveclib=AMDLIBM -z muldefs -mlllvm -unroll-aggressive
-mlllvm -unroll-threshold=500 -lamdlibm -ljemalloc -lflang -lflangrti

Base Other Flags

C benchmarks:
-Wno-unused-command-line-argument

C++ benchmarks:
-Wno-unused-command-line-argument

Peak Compiler Invocation

C benchmarks:
clang

C++ benchmarks:
clang++

Fortran benchmarks:
flang
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Peak Portability Flags

500.perlbench_r -DSPEC_LINUX_X64 -DSPEC_LP64
502.gcc_r -D_FILE_OFFSET_BITS=64
505.mcf_r -DSPEC_LP64
520.omnetpp_r -DSPEC_LP64
523.xalancbmk_r -DSPEC_LINUX -DSPEC_LP64
525.x264_r -DSPEC_LP64
531.deepsjeng_r -DSPEC_LP64
541.leela_r -DSPEC_LP64
548.exchange2_r -DSPEC_LP64
557.xz_r -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r -m64 -Wl,-allow-multiple-definition
-Wl,-mlllvm -Wl,-enable-limm-vrp -flto
-Wl,-mlllvm -Wl,-function-specialize
-Wl,-mlllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mlllvm -Wl,-reduce-array-computations=3
-ffprofile-instr-generate(pass 1)
-ffreprof-instr-use(pass 2) -Ofast -march=znver3
-fveclib=AMDLIBM -fstruct-layout=7
-funroll-loops=50 -fremap-arrays
-mllvm -function-specialization -mlllvm -inline-threshold=1000
-mllvm -enable-gvn-hoist -mlllvm -global-vectorize-slp=false
-mllvm -function-specialize -mlllvm -enable-limm-vrp
-mlllvm -reduce-array-computations=3 -lamdlibm -ljemalloc

502.gcc_r -m32 -Wl,-allow-multiple-definition
-Wl,-mlllvm -Wl,-enable-limm-vrp -flto
-Wl,-mlllvm -Wl,-function-specialize -Ofast -march=znver3
-fveclib=AMDLIBM -fstruct-layout=7
-mlllvm -unroll-threshold=50 -fremap-arrays
-mllvm -function-specialization -mlllvm -inline-threshold=1000
-mllvm -enable-gvn-hoist -mlllvm -global-vectorize-slp=true
-mllvm -function-specialize -mlllvm -enable-limm-vrp

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Peak Optimization Flags (Continued)

502.gcc_r (continued):
-mlvm -reduce-array-computations=3 -fgnu89-inline
-ljemalloc

505.mcf_r: -m64 -Wl,-allow-multiple-definition
-Wl,-mlvm -Wl,-enable-licm-vrp -floom
-Wl,-mlvm -Wl,-function-specialize
-Wl,-mlvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mlvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -fstruct-layout=7
-mlvm -unroll-threshold=1 -fremap-arrays
-flv-function-specialization -mlvm -inline-threshold=1000
-mlvm -enable-gvn-hoist -mlvm -global-vectorize-slp=true
-mlvm -function-specialize -mlvm -enable-licm-vrp
-mlvm -reduce-array-computations=3 -lamdlibm -ljemalloc

525.x264_r: basepeak = yes

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -m64 -std=c++98
-Wl,-mlvm -Wl,-do-block-reorder-aggressive -flto
-Wl,-mlvm -Wl,-function-specialize
-Wl,-mlvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mlvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -finline-aggressive
-mlvm -unroll-threshold=100 -flv-function-specialization
-mlvm -enable-licm-vrp -mlvm -reroll-loops
-mlvm -aggressive-loop-unswitch
-mlvm -reduce-array-computations=3
-mlvm -global-vectorize-slp=true
-mlvm -do-block-reorder-aggressive
-fvirtual-function-elimination -fvisibility=hidden
-lamdlibm -ljemalloc

523.xalancbmk_r: -m32 -Wl,-mlvm -Wl,-do-block-reorder-aggressive -flto
-Wl,-mlvm -Wl,-function-specialize

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Test Date: Jul-2022
Test Sponsor: Cisco Systems
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### Peak Optimization Flags (Continued)

523.xalancbmk_r (continued):
- `-Wl,-mlvm -Wl,-align-all-nofallthru-blocks=6`
- `-Wl,-mlvm -Wl,-reduce-array-computations=3 -Ofast`
- `-march=znver3 -fveclib=AMDLIBM -finline-aggressive`
- `-mlvm -unroll-threshold=100 -flv-function-specialization`
- `-mlvm -enable-licm-vrp -mlvm -reroll-loop`
- `-mlvm -aggressive-loop-unswitch`
- `-mlvm -reduce-array-computations=3`
- `-mlvm -global-vectorize -np=true`
- `-mlvm -do-block-reorder=aggressive`
- `-fvirtual-function-elimination -fvisibility=hidden`
- `-ljemalloc`

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
- `-m64 -Wl,-mlvm -Wl,-inljump-recursion=4`
- `-Wl,-mlvm -Wl, -lslr -lstar -lscatter-loop -Wl,-mlvm -Wl,-enable-iv-splat`
- `-flto -Wl,-mlvm -Wl,-function-specialize`
- `-Wl,-mlvm -Wl,-align-all-nofallthru-blocks=6`
- `-Wl,-mlvm -Wl,-reduce-array-computations=3 -O3 -ffast-math`
- `-march=znver3 -fveclib=AMDLIBM -mlvm -unroll-aggressive`
- `-mlvm -unroll-threshold=500 -landlibm -ljemalloc -lflang -lflangrti`

### Peak Other Flags

C benchmarks (except as noted below):
- `-Wno-unused-command-line-argument`

502.gcc_r: `-L/usr/lib -Wno-unused-command-line-argument`
- `-L/sppo/bin/cpu2017v115aocc3/amd_rate_aocc300_milan_A_lib/32`

C++ benchmarks (except as noted below):
- `-Wno-unused-command-line-argument`

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SPEC CPU®2017 Integer Rate Result

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

SPECrate®2017_int_base =  
SPECrate®2017_int_peak =

Test Date: Jul-2022  
Hardware Availability: Aug-2021  
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CPU2017 License: 9019  
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Hardware Availability: Aug-2021  
Software Availability: Dec-2021

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Software Availability: Dec-2021

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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