SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero IDI100C2R-28
(2.10 GHz, Intel Xeon Silver 4310)

SPECrated®2017_int_base = 176
SPECrated®2017_int_peak = 181

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Sep-2022
Hardware Availability: Apr-2021

Copies

<table>
<thead>
<tr>
<th>Benchmark</th>
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Hardware

CPU Name: Intel Xeon Silver 4310
Max MHz: 3300
Nominal: 2100
Enabled: 24 cores, 2 chips, 2 threads/core
Orderable: 1.2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 18 MB I+D on chip per chip
Other: None
Memory: 1 TB (16 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)
Storage: 1 x 512 GB NVMe SSD
Other: None

Software

OS: Red Hat Enterprise Linux release 8.5 (Ootpa)
Kernel 4.18.0-348.el8.x86_64
Compiler: C/C++: Version 2022.1 of Intel oneAPI DPC++/C++ Compiler for Linux;
Fortran: Version 2022.1 of Intel Fortran Compiler for Linux;
Parallel: No
Firmware: Version SES5C620.86B.01.01.0004.2110190142 released Oct-2021
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage.
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#### Results Table

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

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#### Compiler Notes

SPEC has ruled that the compiler used for this result was performing a compilation that specifically improves the performance of the 523.xalancbmk_r / 623.xalancbmk_s benchmarks using a priori knowledge of the SPEC code and dataset to perform a transformation that has narrow applicability.

In order to encourage optimizations that have wide applicability (see rule 1.4 https://www.spec.org/cpu2017/Docs/runrules.html#rule_1.4), SPEC will no longer publish results using this optimization.

This result is left in the SPEC results database for historical reference.

---

#### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

---

#### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

#### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOC_CONF = "retain:true"
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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

General Notes

Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM
memory using Red Hat Enterprise Linux 8.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the
system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the
system as tested and documented.
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the
system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Power Technology = Custom
ENERGY_PERF_BIAS_CFG mode = Maximum Performance
KTI Prefetch = Enable
LLC Dead Line Alloc = Enable
Hyper-Threading = Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf0b6d
running on icelakespec Thu Sep 1 08:03:01 2022

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4310 CPU @ 2.10GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 24
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11

From lscpu from util-linux 2.32.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 12
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
BIOS Vendor ID: Intel(R) Corporation
CPU family: 6

(Continued on next page)
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CPU2017 License: 006042
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Tested by: Tyrone Systems

Test Date: Sep-2022
Hardware Availability: Apr-2021
Software Availability: May-2022

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Platform Notes (Continued)

Model: 106
Model name: Intel(R) Xeon(R) Silver 4310 CPU @ 2.10GHz
BIOS Model name: Intel(R) Xeon(R) Silver 4310 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000
CPU max MHz: 3300.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 18432K
NUMA node0 CPU(s): 0-5,24-29
NUMA node1 CPU(s): 6-11,30-35
NUMA node2 CPU(s): 12-17,36-41
NUMA node3 CPU(s): 18-23,42-47
Flags: fpu vme de pse tsc msr pae mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl x87fpu wp vs mpx pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
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pat

/proc/cpuinfo cache data

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 24 25 26 27 28 29
node 0 size: 257632 MB
node 0 free: 256792 MB
node 1 cpus: 6 7 8 9 10 11 30 31 32 33 34 35
node 1 size: 258045 MB
node 1 free: 257612 MB
node 2 cpus: 12 13 14 15 16 17 36 37 38 39 40 41
node 2 size: 258045 MB
node 2 free: 257748 MB
node 3 cpus: 18 19 20 21 22 23 42 43 44 45 46 47
node 3 size: 258042 MB
node 3 free: 257716 MB
node distances:
node 0 1 2 3
0: 10 11 20 20
1: 11 10 20 20
2: 20 20 10 11
3: 20 20 11 10

From /proc/meminfo
MemTotal: 1056528044 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

(Continued on next page)
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<td>Software Availability: May-2022</td>
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Platform Notes (Continued)

/sbin/tuned-adm active
  Current active profile: throughput-performance
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*, /etc/*version*
  os-release:
    NAME="Red Hat Enterprise Linux"
    VERSION="8.5 (Ootpa)"
    ID="rhel"
    ID_LIKE="fedora"
    VERSION_ID="8.5"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="Red Hat Enterprise Linux 8.5 (Ootpa)"
    ANSI_COLOR="0;31"

  redhat-release: Red Hat Enterprise Linux release 8.5 (Ootpa)
  system-release: Red Hat Enterprise Linux release 8.5 (Ootpa)
  system-release-cpe: cpe:/o:redhat:enterprise_linux:8::baseos

uname -a:
  Linux icelakespec 4.18.0-348.el8.x86_64 #1 SMP Mon Oct 4 12:17:22 EDT 2021 x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass):
  Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: Speculative Store
  barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):
  Mitigation: Enhanced IBRS, IBPB:
    conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Sep 1 08:01

SPEC is set to: /home/cpu2017

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
  16x Samsung M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

(Continued on next page)
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**Test Sponsor:** Netweb Pte Ltd  
**Tested by:** Tyrone Systems

**Platform Notes (Continued)**

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| BIOS Vendor: Intel Corporation  
| BIOS Version: SE5C620.86B.01.01.0004.2110190142  
| BIOS Date: 10/19/2021 |

(End of data from sysinfo program)

**Compiler Version Notes**

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Copyright 2017-2024 Standard Performance Evaluation Corporation

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Software Availability: May-2022

Test Date: Sep-2022
Hardware Availability: Apr-2021

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifx

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-ll/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-ll/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-ll/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin
-lqkmalloc
## Peak Compiler Invocation

**C benchmarks:**
- icx

**C++ benchmarks:**
- icpx

**Fortran benchmarks:**
- ifx

## Peak Portability Flags

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<td>-DSPEC_LP64 -DSPEC_LINUX_X64</td>
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<tr>
<td>502.gcc_r</td>
<td>-D_FILE_OFFSET_BITS=64</td>
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<tr>
<td>505.mcf_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX</td>
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<tr>
<td>525.x264_r</td>
<td>-DSPEC_LP64</td>
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<tr>
<td>531.deepsjeng_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

## Peak Optimization Flags

**C benchmarks:**

```bash
500.perlbench_r: -w -std=c11 -m64 -Wl,-z,muldefs
-fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2 -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -fno-strict-overflow
-L/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin
-lqkmalloc
```

```bash
502.gcc_r: -m32
-L/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2 -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -L/usr/local/jemalloc32-5.0.1/lib
-ljemalloc
```

(Continued on next page)
### SPEC CPU®2017 Integer Rate Result

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
**Tyrone Camarero IDI100C2R-28**  
(2.10 GHz, Intel Xeon Silver 4310)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 176</th>
<th>Test Date: Sep-2022</th>
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<tbody>
<tr>
<td>SPECrate®2017_int_peak = 181</td>
<td>Hardware Availability: Apr-2021</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 006042  
**Test Sponsor:** Netweb Pte Ltd  
**Tested by:** Tyrone Systems

#### Peak Optimization Flags (Continued)

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast  
-ffast-math -flto -mfpmath=sse -funroll-loops  
-qopt-mem-layout-trans=4 -fno-alias  
-L/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin  
-lqkmalloc

557.xz_r: basepeak = yes

C++ benchmarks:

520.omnetpp_r: basepeak = yes  
523.xalancbmk_r: basepeak = yes  
531.deepsjeng_r: basepeak = yes  
541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-ICX-revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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