## SPEC CPU®2017 Integer Rate Result

Tyrone Systems  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero TDI100C3R-212  
(2.40 GHz, Intel Xeon Silver 4314)

**SPECrates**  
- **SPECrates**
- **SPECrates**

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Sep-2022</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2021</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2022</td>
</tr>
</tbody>
</table>

- **CPU2017 License:** 006042  
- **Test Sponsor:** Netweb Pte Ltd  
- **Tested by:** Tyrone Systems  

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>64</td>
<td>(225)</td>
<td>(219)</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Silver 4314  
- **Max MHz:** 3400  
- **Nominal:** 2400  
- **Enabled:** 32 cores, 2 chips, 2 threads/core  
- **Orderable:** 1.2 Chips  
- **Cache L1:** 32 KB I + 48 KB D on chip per core  
- **L2:** 1.25 MB I+D on chip per core  
- **L3:** 24 MB I+D on chip per core  
- **Other:** None  
- **Memory:** 1 TB (16 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)  
- **Storage:** 1 x 512 GB NVMe SSD  
- **Other:** None

### Software

- **OS:** Red Hat Enterprise Linux release 8.5 (Ootpa) 4.18.0-348.el8.x86_64  
- **Compiler:** C/C++: Version 2022.1 of Intel oneAPI DPC++/C++ Compiler for Linux; Fortran: Version 2022.1 of Intel Fortran Compiler for Linux;  
- **Parallel:** No  
- **Firmware:** Version PEGC0020 released Aug-2022  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage.
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero TDI100C3R-212
(2.40 GHz, Intel Xeon Silver 4314)

SPECrate®2017_int_base = 219
SPECrate®2017_int_peak = 225

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Base Copies</th>
<th>Base Seconds</th>
<th>Base Ratio</th>
<th>Peak Copies</th>
<th>Peak Seconds</th>
<th>Peak Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>64</td>
<td>699</td>
<td>146</td>
<td>64</td>
<td>646</td>
<td>158</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>64</td>
<td>525</td>
<td>173</td>
<td>64</td>
<td>464</td>
<td>195</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>64</td>
<td>301</td>
<td>343</td>
<td>64</td>
<td>301</td>
<td>343</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>64</td>
<td>596</td>
<td>141</td>
<td>64</td>
<td>596</td>
<td>141</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>64</td>
<td>204</td>
<td>332</td>
<td>64</td>
<td>204</td>
<td>332</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>64</td>
<td>255</td>
<td>141</td>
<td>64</td>
<td>255</td>
<td>141</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>64</td>
<td>450</td>
<td>163</td>
<td>64</td>
<td>450</td>
<td>163</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>64</td>
<td>645</td>
<td>144</td>
<td>64</td>
<td>645</td>
<td>144</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>64</td>
<td>349</td>
<td>481</td>
<td>64</td>
<td>349</td>
<td>481</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>64</td>
<td>595</td>
<td>116</td>
<td>64</td>
<td>595</td>
<td>116</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

SPEC has ruled that the compiler used for this result was performing a compilation that specifically improves the performance of the 523.xalancbmk_r / 623.xalanchmk_s benchmarks using a priori knowledge of the SPEC code and dataset to perform a transformation that has narrow applicability.

In order to encourage optimizations that have wide applicability (see rule 1.4 https://www.spec.org/cpu2017/Docs/runrules.html#rule_1.4), SPEC will no longer publish results using this optimization.

This result is left in the SPEC results database for historical reference.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero TDI100C3R-212
(2.40 GHz, Intel Xeon Silver 4314)

SPECrate®2017_int_base = 219
SPECrate®2017_int_peak = 225

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems
Test Date: Sep-2022
Hardware Availability: Apr-2021
Software Availability: May-2022

General Notes
Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM
memory using Red Hat Enterprise Linux 8.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.: 
numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes
BIOS Settings:
Power Technology = Custom
ENERGY_PERF_BIAS_CFG mode = Performance
KTI Prefetch = Enable
LLC Dead Line Alloc = Disable
Hyper-Threading = Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on Tyrone spec Thu Sep 1 17:38:24 2022

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu from util-linux 2.32.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
BIOS Vendor ID: Intel(R) Corporation
CPU family: 6
SPEC CPU®2017 Integer Rate Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero TDI100C3R-212
(2.40 GHz, Intel Xeon Silver 4314)

SPECrate®2017_int_base = 219
SPECrate®2017_int_peak = 225

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Sep-2022
Hardware Availability: Apr-2021
Software Availability: May-2022

Platform Notes (Continued)

Model: 106
Model name: Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
BIOS Model name: Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
Stepping: 6
CPU MHz: 2400.000
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 24576K
NUMA node0 CPU(s): 0-15,32-47
NUMA node1 CPU(s): 16-31,48-63
Flags: fpu vme de pse tsc msr pme mca cmov pat pse36 cdflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperf perfctr npt cpuid_fault epb cat_13 invpcid_single intel_pni sbbp mba ibsf ibpb ibrs enhanced tpr_shadow vmx flexpriority ept vpid ept_ad fsgsbase tsc_adjust sgx bmi1 hle avx2 smep bmi2 erms invpcid cqm rdt_a avx512f avx512dq rdseed adx smap avx512sfma clflushopt clwb intel_pt avx512cd sha_nl avx512bw avx512vl xsaveopt xsavevc saxseg xsaveprec xsaves cqm_l1c cqm_mbb_total cqm_mbb_local split_lock_detect wbinvd dtherm ida arat pin pts hwp hwp_act_window hwp_epp hwp_pkeq axv512vbm umip pku ospke avx512_vbmi2 gfnl vaes vpcmimdq avx512_wwi avx512_bitalg tme avx512 vpocntdq la57 rdpid sgp lc fasm md_clear pconf gflush l1d arch_capabilities

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 32 33 34 35 36 37 38 39 40 41 42 43
44 45 46 47
node 0 size: 515642 MB
node 0 free: 514931 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 48 49 50 51 52 53 54 55 56
57 58 59 60 61 62 63
node 1 size: 516086 MB
node 1 free: 516086 MB
node distances:
node 0 1
0: 10 20
1: 20 10

From /proc/meminfo
MemTotal: 1056490608 kB
MemFree: 515642 MB
MemAvailable: 514931 MB
MemDispersed: 1047037432 kB

From /sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

(Continued on next page)
Platform Notes (Continued)

From /etc/*release* /etc/*version*
  os-release:
    NAME="Red Hat Enterprise Linux"
    VERSION="8.5 (Ootpa)"
    ID="rhel"
    ID_LIKE="fedora"
    VERSION_ID="8.5"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="Red Hat Enterprise Linux 8.5 (Ootpa)"
    ANSI_COLOR="0;31"
  redhat-release: Red Hat Enterprise Linux release 8.5 (Ootpa)
  system-release: Red Hat Enterprise Linux release 8.5 (Ootpa)
  system-release-cpe: cpe:/o:redhat:enterprise_linux:8::baseos

uname -a:
  Linux Tyronespec 4.18.0-348.el8.x86_64 #1 SMP Mon Oct 4 12:17:22 EDT 2021 x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Sep 1 17:33

SPEC is set to: /home/cpu2017

Filesystem       Type      Size  Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs   402G  130G  272G  33% /home

From /sys/devices/virtual/dmi/id
  Vendor:           Tyrone Systems
  Product:          Tyrone Camarero TDI100C3R-212
  Product Family:   Family
  Serial:           2X22002203

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
  16x Samsung M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
  BIOS Vendor: American Megatrends International, LLC.
  BIOS Version: PEGC0020
  BIOS Date:   08/12/2022
  BIOS Revision: 5.22
SPEC CPU®2017 Integer Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero TDI100C3R-212
(2.40 GHz, Intel Xeon Silver 4314)

SPECrate®2017_int_base = 219
SPECrate®2017_int_peak = 225

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Sep-2022
Hardware Availability: Apr-2021
Software Availability: May-2022

Platform Notes (Continued)

(End of data from sysinfo program)

Compiler Version Notes

============================================================================================================
C | 502.gcc_r(peak)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

============================================================================================================
C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak)
557.xz_r(base, peak)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

============================================================================================================
C | 502.gcc_r(peak)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

============================================================================================================
C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak)
557.xz_r(base, peak)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

============================================================================================================
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak) 531.deepsjeng_r(base, peak)
541.leela_r(base, peak)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

============================================================================================================
Fortran | 548.exchange2_r(base, peak)
Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx

(Continued on next page)
# SPEC CPU®2017 Integer Rate Result

## Base Compiler Invocation (Continued)

<table>
<thead>
<tr>
<th>Base Portability Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>C++ benchmarks:</td>
</tr>
<tr>
<td>icpx</td>
</tr>
<tr>
<td>Fortran benchmarks:</td>
</tr>
<tr>
<td>ifx</td>
</tr>
</tbody>
</table>

## Base Optimization Flags

<table>
<thead>
<tr>
<th>C benchmarks:</th>
</tr>
</thead>
<tbody>
<tr>
<td>-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ffast-math -flto</td>
</tr>
<tr>
<td>-mfpmath=ssse -funroll-loops -qopt-mem-layout-trans=4</td>
</tr>
<tr>
<td>-L/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin</td>
</tr>
<tr>
<td>-lqkmalloc</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>C++ benchmarks:</th>
</tr>
</thead>
<tbody>
<tr>
<td>-w -m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ffast-math -flto</td>
</tr>
<tr>
<td>-mfpmath=ssse -funroll-loops -qopt-mem-layout-trans=4</td>
</tr>
<tr>
<td>-L/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin</td>
</tr>
<tr>
<td>-lqkmalloc</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fortran benchmarks:</th>
</tr>
</thead>
<tbody>
<tr>
<td>-w -m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ffast-math -flto</td>
</tr>
<tr>
<td>-mfpmath=ssse -funroll-loops -qopt-mem-layout-trans=4</td>
</tr>
<tr>
<td>-nostandard-realloc-lhs -align array32byte -auto</td>
</tr>
<tr>
<td>-L/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin</td>
</tr>
<tr>
<td>-lqkmalloc</td>
</tr>
</tbody>
</table>
SPEC CPU®2017 Integer Rate Result
Copyright 2017-2024 Standard Performance Evaluation Corporation

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero TDI100C3R-212
(2.40 GHz, Intel Xeon Silver 4314)  

SPEC®2017_int_base = 219
SPEC®2017_int_peak = 225

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Peak Compiler Invocation

C benchmarks:
icx
C++ benchmarks:
icpx
Fortran benchmarks:
ifx

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -w -std=c11 -m64 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2 -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -fno-strict-overflow
-L/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2 -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -L/usr/local/jemalloc32-5.0.1/lib
-ljemalloc

(Continued on next page)
Peak Optimization Flags (Continued)

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: basepeak = yes

C++ benchmarks:

520.omnetpp_r: basepeak = yes
523.xalancbmk_r: basepeak = yes
531.deepsjeng_r: basepeak = yes
541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-ICX-revA.xml

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2022-09-01 08:08:24-0400.
Report generated on 2024-01-29 17:06:33 by CPU2017 PDF formatter v6716.
Originally published on 2022-09-27.