SPEC CPU®2017 Integer Speed Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero SDI100A3U-212
(2.90 GHz, Intel Xeon Gold 6326)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base = 9.97</th>
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<tr>
<td>SPECspeed®2017_int_peak = 10.1</td>
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Tyrone Systems
(2.90 GHz, Intel Xeon Gold 6326)

CPU 2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

**CPU Name:** Intel Xeon Gold 6326
**Max MHz:** 3500
**Nominal:** 2900

**Enabled:** 32 cores, 2 chips, 2 threads/core
**Orderable:** 1.2 chips

**Cache L1:** 32 KB I + 48 KB D on chip per core
**L2:** 1.25 MB I+D on chip per core
**L3:** 24 MB I+D on chip per core

**Other:** None
**Memory:** 1 TB (16 x 64 GB 2Rx4 PC4-3200AA-R)
**Storage:** 1 x 512 GB NVMem SSD

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<td>Compiler: C/C++: Version 2022.1 of Intel oneAPI DPC++/C++ Compiler for Linux; Fortran: Version 2022.1 of Intel Fortran Compiler for Linux;</td>
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<td>Parallel: Yes</td>
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<td>Firmware: Version 1.2a released May-2022</td>
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<td>File System: xfs</td>
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<td>System State: Run level 3 (multi-user)</td>
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<td>Base Pointers: 64-bit</td>
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## Results Table

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<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
<td>600.perlbench_s</td>
<td>64</td>
<td>304</td>
<td>5.83</td>
<td>303</td>
<td>5.86</td>
<td>302</td>
<td>5.88</td>
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<tr>
<td>605.mcf_s</td>
<td>64</td>
<td>278</td>
<td>17.0</td>
<td>278</td>
<td>17.0</td>
<td>278</td>
<td>17.0</td>
<td>64</td>
<td>278</td>
<td>17.0</td>
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<tr>
<td>620.omnetpp_s</td>
<td>64</td>
<td>259</td>
<td>6.30</td>
<td>257</td>
<td>6.34</td>
<td>257</td>
<td>6.33</td>
<td>64</td>
<td>259</td>
<td>6.30</td>
<td>257</td>
<td>6.34</td>
<td>257</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>64</td>
<td>80.7</td>
<td>17.6</td>
<td>79.9</td>
<td>17.7</td>
<td>80.4</td>
<td>17.6</td>
<td>64</td>
<td>80.7</td>
<td>17.6</td>
<td>79.9</td>
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<td>80.4</td>
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<tr>
<td>625.x264_s</td>
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<td>14.1</td>
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<td>14.2</td>
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<td>631.deepsjeng_s</td>
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<td>4.94</td>
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<td>290</td>
<td>4.94</td>
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</tr>
<tr>
<td>641.leela_s</td>
<td>64</td>
<td>423</td>
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<td>423</td>
<td>4.03</td>
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<td>423</td>
<td>4.03</td>
<td>423</td>
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<td>423</td>
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<tr>
<td>648.exchange2_s</td>
<td>64</td>
<td>177</td>
<td>16.6</td>
<td>177</td>
<td>16.6</td>
<td>177</td>
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<td>64</td>
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<td>16.6</td>
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<td>657.xz_s</td>
<td>64</td>
<td>303</td>
<td>20.3</td>
<td>304</td>
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**SPECspeed®2017_int_base = 9.97**

**SPECspeed®2017_int_peak = 10.1**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Compiler Notes

SPEC has ruled that the compiler used for this result was performing a compilation that specifically improves the performance of the 523.xalanchmk_r / 623.xalanchmk_s benchmarks using a priori knowledge of the SPEC code and dataset to perform a transformation that has narrow applicability.

In order to encourage optimizations that have wide applicability (see rule 1.4 https://www.spec.org/cpu2017/Docs/runrules.html#rule_1.4), SPEC will no longer publish results using this optimization.

This result is left in the SPEC results database for historical reference.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/jd5.0.1-64"
- MALLOC_CONF = "retain:true"
- OMP_STACKSIZE = "192M"
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---

**General Notes**

Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM
memory using Red Hat Enterprise Linux 8.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
\texttt{sync; echo 3>/proc/sys/vm/drop_caches}
runcpu command invoked through numactl i.e.:
\texttt{numactl --interleave=all runcpu <etc>}

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

---

**Platform Notes**

BIOS Settings:
- Power Technology = Custom
- ENERGY_PERF_BIAS_CFG mode = Maximum Performance
- SNC (Sub NUMA)= Enable
- KTI Prefetch= Enable
- LLC Dead Line Alloc = Disable
- Hyper-Threading = Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b5581ef0e16acaf64d
running on icelake2 Sat Oct 8 13:07:57 2022

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
\texttt{model name : Intel(R) Xeon(R) Gold 6326 CPU @ 2.90GHz}
\texttt{2 "physical Id"s (chips)}
\texttt{64 "processors"}
\texttt{cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)}
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lsccpu from util-linux 2.32.1:
\texttt{Architecture: x86_64}
\texttt{CPU op-mode(s): 32-bit, 64-bit}
\texttt{Byte Order: Little Endian}
\texttt{CPU(s): 64}
\texttt{On-line CPU(s) list: 0-63}
\texttt{Thread(s) per core: 2}
\texttt{Core(s) per socket: 16}
\texttt{Socket(s): 2}
\texttt{NUMA node(s): 4}
\texttt{Vendor ID: GenuineIntel}
\texttt{BIOS Vendor ID: Intel(R) Corporation}

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### CPU2017 License: 006042  
Test Sponsor: Netweb Pte Ltd  
Tested by: Tyrone Systems  

### Platform Notes (Continued)

- **CPU family:** 6  
- **Model:** 106  
- **Model name:** Intel(R) Xeon(R) Gold 6326 CPU @ 2.90GHz  
- **Stepping:** 6  
- **CPU MHz:** 2900.000  
- **BogoMIPS:** 5800.00  
- **Virtualization:** VT-x  

### L1d cache: 48K  
### L1i cache: 32K  
### L2 cache: 1280K  
### L3 cache: 24576K  

<table>
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<tr>
<th>NUMA node0 CPU(s):</th>
<th>0-7, 32-39</th>
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<tr>
<td>NUMA node1 CPU(s):</td>
<td>8-15, 40-47</td>
</tr>
<tr>
<td>NUMA node2 CPU(s):</td>
<td>16-23, 48-55</td>
</tr>
<tr>
<td>NUMA node3 CPU(s):</td>
<td>24-31, 56-63</td>
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</table>

### Flags:
- fpu  
- vme  
- de  
- pse  
- tsc  
- msr  
- pae  
- mce  
- cx8  
- apic  
- sep  
- mtrr  
- pge  
- mca  
- cmov  
- pat  
- pse36  
- clflush  
- dts  
- acpi  
- fxsrv  
- sse  
- sse2  
- ss  
- ht  
- tm  
- pbe  

### /proc/cpuinfo cache data  
- cache size: 24576 KB

From numactl --hardware  
WARNING: a numactl 'node' might or might not correspond to a physical chip.

### From /proc/meminfo  
- MemTotal: 1056487912 kB  
- HugePages_Total: 0  
- Hugepagesize: 2048 kB

(Continued on next page)
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Test Sponsor: Netweb Pte Ltd  
Tested by: Tyrone Systems  
Test Date: Oct-2022  
Hardware Availability: Jun-2021  
Software Availability: May-2022

---

### Platform Notes (Continued)

```
/sbin/tuned-adm active
Current active profile: throughput-performance
```

```
From /etc/*release* /etc/*version*
```

```
NAME="Red Hat Enterprise Linux"
VERSION="8.5 (Ootpa)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="8.5"
PLATFORM_ID="platform:e18"
PRETTY_NAME="Red Hat Enterprise Linux 8.5 (Ootpa)"
ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.5 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.5 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8::baseos
```

```
uname -a:
Linux icelake2 4.18.0-348.el8.x86_64 #1 SMP Mon Oct 4 12:17:22 EDT 2021 x86_64 x86_64
x86_64 GNU/Linux
```

```
Kernel self-reported vulnerability status:
```

CVE-2018-12207 (iTLB Multihit): Not affected  
CVE-2018-3620 (L1 Terminal Fault): Not affected  
Microarchitectural Data Sampling: Not affected  
CVE-2017-5754 (Meltdown): Not affected  
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp  
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps barriers and __user pointer sanitization  
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling  
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected  
CVE-2019-11135 (TSX Asynchronous Abort): Not affected  

run-level 3 Oct 6 11:21
```

SPEC is set to: /home/cpu2017  
Filesystem Type Size Used Avail Use% Mounted on  
/dev/mapper/rhel-home xfs 402G 156G 247G 39% /home

From /sys/devices/virtual/dmi/id
Vendor: Tyrone Systems  
Product: Tyrone Camarero SDI100A3U-212  
Product Family: SMC X12

```
Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
```

```
Memory:
16x Samsung M393A8G40AB2-CWE 64 GB 2 rank 3200
```

```
BIOS:
BIOS Vendor: American Megatrends International, LLC.
BIOS Version: 1.2a
BIOS Date: 05/12/2022
```

(Continued on next page)
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<td>Tested by: Tyrone Systems</td>
<td>Software Availability: May-2022</td>
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Platform Notes (Continued)

BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

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<tr>
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

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<th>C++</th>
<th>620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak)</th>
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

| Fortran     | 648.exchange2_s(base, peak)                                                      |

Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifx

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64

(Continued on next page)
Base Portability Flags (Continued)

631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -g -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -fiopenmp
-DSPEC_OPENMP -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

C++ benchmarks:
-m64 -g -Wl,-z,muldefs -xCORE-AVX2 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:
-m64 -g -Wl,-z,muldefs -xCORE-AVX2 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifx

Peak Portability Flags

Same as Base Portability Flags
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Peak Optimization Flags

C benchmarks:

600.perlbench_s: -m64 -g -std=c11 -Wl, -z, muldefs
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -fiopenmp -DSPEC_OPENMP
-fno-strict-overflow -L/usr/local/jemalloc64-5.0.1/lib
-ljemalloc

602.gcc_s: -m64 -g -std=c11 -Wl, -z, muldefs
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -fiopenmp -DSPEC_OPENMP
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

605.mcf_s: basepeak = yes

625.x264_s: -m64 -g -std=c11 -Wl, -z, muldefs -xCORE-AVX2 -O3
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -fiopenmp -DSPEC_OPENMP
-fno-alias -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

657.xz_s: basepeak = yes

C++ benchmarks:

620.omnetpp_s: basepeak = yes

Fortran benchmarks:

648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at
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You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-ICX-revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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