# SPEC CPU® 2017 Integer Rate Result

## Cisco Systems

Cisco UCS C245 M6 (AMD EPYC 7282 16-core Processor)

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>64</td>
<td>219</td>
<td>240</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Date:** Oct-2022  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Aug-2021  
**Tested by:** Cisco Systems  
**Software Availability:** Dec-2021

### Hardware

- **CPU Name:** AMD EPYC 7282  
- **Max MHz:** 3200  
- **Nominal:** 2800  
- **Enabled:** 32 cores, 2 chips, 2 threads/core  
- **Orderable:** 1.2 chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 512 KB I+D on chip per core  
- **L3:** 64 MB I+D on chip per chip, 16 MB shared / 4 cores  
- **Other:** None  
- **Memory:** 2 TB (16 x 128 GB 4Rx4 PC4-3200AA-L)  
- **Storage:** 1 x 960 GB M.2 SSD SATA  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 SP3 (x86_64)  
- **Compiler:** C/C++/Fortran: Version 3.2.0 of AOCC  
- **Parallel:** No  
- **Firmware:** Version 4.2.2b released May-2022  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc: jemalloc memory allocator library v5.1.0  
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C245 M6 (AMD EPYC 7282 16-core Processor)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2022
Hardware Availability: Aug-2021
Software Availability: Dec-2021

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>64</td>
<td>608</td>
<td>168</td>
<td>610</td>
<td>167</td>
<td>607</td>
<td>168</td>
<td>608</td>
<td>168</td>
<td>610</td>
<td>167</td>
<td>607</td>
<td>168</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>64</td>
<td>521</td>
<td>174</td>
<td>518</td>
<td>175</td>
<td>517</td>
<td>175</td>
<td>406</td>
<td>223</td>
<td>406</td>
<td>223</td>
<td>407</td>
<td>223</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>64</td>
<td>308</td>
<td>336</td>
<td>308</td>
<td>336</td>
<td>308</td>
<td>335</td>
<td>296</td>
<td>349</td>
<td>295</td>
<td>351</td>
<td>296</td>
<td>350</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>64</td>
<td>823</td>
<td>102</td>
<td>823</td>
<td>102</td>
<td>822</td>
<td>102</td>
<td>823</td>
<td>102</td>
<td>822</td>
<td>102</td>
<td>296</td>
<td>350</td>
</tr>
<tr>
<td>523.xalanbm_k_r</td>
<td>64</td>
<td>395</td>
<td>171</td>
<td>393</td>
<td>172</td>
<td>395</td>
<td>171</td>
<td>215</td>
<td>315</td>
<td>217</td>
<td>311</td>
<td>215</td>
<td>315</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>64</td>
<td>222</td>
<td>504</td>
<td>221</td>
<td>507</td>
<td>222</td>
<td>505</td>
<td>222</td>
<td>505</td>
<td>222</td>
<td>505</td>
<td>222</td>
<td>505</td>
</tr>
<tr>
<td>531.deepsjang_r</td>
<td>64</td>
<td>365</td>
<td>201</td>
<td>364</td>
<td>201</td>
<td>365</td>
<td>201</td>
<td>365</td>
<td>201</td>
<td>364</td>
<td>201</td>
<td>364</td>
<td>201</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>64</td>
<td>549</td>
<td>193</td>
<td>549</td>
<td>193</td>
<td>550</td>
<td>193</td>
<td>546</td>
<td>194</td>
<td>546</td>
<td>194</td>
<td>546</td>
<td>194</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>64</td>
<td>298</td>
<td>562</td>
<td>301</td>
<td>557</td>
<td>307</td>
<td>546</td>
<td>297</td>
<td>564</td>
<td>298</td>
<td>562</td>
<td>297</td>
<td>564</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>64</td>
<td>517</td>
<td>134</td>
<td>517</td>
<td>134</td>
<td>518</td>
<td>134</td>
<td>517</td>
<td>134</td>
<td>517</td>
<td>134</td>
<td>518</td>
<td>134</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The AMD64 AOCC Compiler Suite is available at http://developer.amd.com/amd-aocc/

Submit Notes

The config file option 'submit' was used.
'numactl' was used to bind copies to the cores.
See the configuration file for details.

Operating System Notes

'ulimit -s unlimited' was used to set environment stack size limit
'ulimit -l 2097152' was used to set environment locked pages in memory limit

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

To limit dirty cache to 8% of memory, 'sysctl -w vm.dirty_ratio=8' run as root.
To limit swap usage to minimum necessary, 'sysctl -w vm.swappiness=1' run as root.
To free node-local memory and avoid remote memory usage, 'sysctl -w vm.zone_reclaim_mode=1' run as root.
To clear filesystem caches, 'sync; sysctl -w vm.drop_caches=3' run as root.
To disable address space layout randomization (ASLR) to reduce run-to-run variability, 'sysctl -w kernel.randomize_va_space=0' run as root.

(Continued on next page)
Cisco Systems
Cisco UCS C245 M6 (AMD EPYC 7282 16-core Processor)

Operating System Notes (Continued)

To enable Transparent Hugepages (THP) only on request for base runs,
'echo madvise > /sys/kernel/mm/transparent_hugepage/enabled' run as root.
To enable THP for all allocations for peak runs,
'echo always > /sys/kernel/mm/transparent_hugepage/enabled' and
'echo always > /sys/kernel/mm/transparent_hugepage/defrag' run as root.

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
    "/home/cpu2017/amd_rate_aocc320_milanx_A_lib/lib;/home/cpu2017/amd_rate_aocc320_milanx_A_lib/lib32:"
MALLOCP_CONF = "retain:true"

Environment variables set by runcpu during the 523.xalancbmk_r peak run:
MALLOCP_CONF = "thp:never"

General Notes

Binaries were compiled on a system with 2x AMD EPYC 7742 CPU + 1TiB Memory using OpenSUSE 15.2

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc: configured and built with GCC v4.8.2 in RHEL 7.4 (No options specified)
jemalloc 5.1.0 is available here:
https://github.com/jemalloc/jemalloc/releases/download/5.1.0/jemalloc-5.1.0.tar.bz2

Platform Notes

SMT Mode set to Enabled
NUMA nodes per socket set to NPS4
ACPI SRAT L3 Cache As NUMA Domain set to Enabled
DRAM Scrub Time set to Disabled
Determinism Slider set to Power
Memory Interleaving set to Disabled
APBDIS set to 1

(Continued on next page)
Platform Notes (Continued)

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acac64d
running on SPEC-SRV02 Mon Oct 24 05:51:39 2022

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
   https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
   model name : AMD EPYC 7282 16-Core Processor
   2 "physical id"s (chips)
   64 "processors"
   cores, siblings (Caution: counting these is hw and system dependent. The following
   excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
   cpu cores : 16
   siblings : 32
   physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
   physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu from util-linux 2.36.2:
   Architecture:            x86_64
   CPU op-mode(s):          32-bit, 64-bit
   Byte Order:              Little Endian
   Address sizes:           43 bits physical, 48 bits virtual
   CPU(s):                  64
   On-line CPU(s) list:     0-63
   Thread(s) per core:      2
   Core(s) per socket:      16
   Socket(s):               2
   NUMA node(s):            8
   Vendor ID:               AuthenticAMD
   CPU family:              23
   Model:                   49
   Model name:              AMD EPYC 7282 16-Core Processor
   Stepping:                0
   Frequency boost:         enabled
   CPU MHz:                 1843.748
   CPU max MHz:             2800.0000
   CPU min MHz:             1500.0000
   BogoMIPS:                5589.76
   Virtualization:         AMD-V
   L1d cache:               1 MiB
   L1i cache:               1 MiB
   L2 cache:                16 MiB
   L3 cache:                128 MiB
   NUMA node0 CPU(s):      0-3,32-35

(Continued on next page)
Cisco Systems  
Cisco UCS C245 M6 (AMD EPYC 7282 16-core) Processor

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Oct-2022</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Aug-2021</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Dec-2021</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base = 219**

**SPECrate®2017_int_peak = 240**

---

**Platform Notes (Continued)**

NUMA node1 CPU(s): 4-7, 36-39
NUMA node2 CPU(s): 8-11, 40-43
NUMA node3 CPU(s): 12-15, 44-47
NUMA node4 CPU(s): 16-19, 48-51
NUMA node5 CPU(s): 20-23, 52-55
NUMA node6 CPU(s): 24-27, 56-59
NUMA node7 CPU(s): 28-31, 60-63

Vulnerability Itlb multihit: Not affected
Vulnerability Ltf: Not affected
Vulnerability Mds: Not affected
Vulnerability Meltdown: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitization
Vulnerability Spectre v2: Mitigation; Full AMD retpoline, IBPF conditional, IBRS_FW, STIBP conditional, RSB filling
Vulnerability Srbds: Not affected
Vulnerability Tsx async abort: Not affected

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush mmx fxsr sse sse2 ht syscall nx mmxext fxsr_opt pdpe1gb rdsc$v cpl_tsc rep_good nopl nonstop_tsc cpuid extd_apicid aperfmperf pni pclmulqdq monitor ssse3 fma cx16 sse4_1 sse4_2 movbe popcnt aes xsave avx f16c rdrand lahf_lm cmp_legacy svm extapic cr8_legacy abm sse4a misalignsse 3dnowprefetch osvw ibr sskinht wdt tce topoext perfctr_core perfctr_nb bpxe perfctr_l1c mwaltx cpb cat_l3 cdnp_l3 hw_pstate sme ssbd mba sev ibrs ibpb stibp vmmcall sev_es fs_base bni avx2 smep bmi2 cqm rdt_a rdseed adx smap clflushopt clwb sha_ni xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local clzero irperf xsaveopt wbnoinvd arat npt lbv svm_lock nrip_save tscc_scale vmcb_clean flushbyasid decodeassists pausefilter pfthreshold avic v_vmsave VMload vgfi umip rpdpd overflow_recover succor smca

From lscpu --cache:

<table>
<thead>
<tr>
<th>NAME</th>
<th>ONE-SIZE</th>
<th>ALL-SIZE</th>
<th>WAYS</th>
<th>TYPE</th>
<th>LEVEL</th>
<th>SETS</th>
<th>PHY-LINE</th>
<th>COHERENCY-SIZE</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1d</td>
<td>32K</td>
<td>1M</td>
<td>8</td>
<td>Data</td>
<td>1</td>
<td>64</td>
<td>1</td>
<td>64</td>
</tr>
<tr>
<td>L1i</td>
<td>32K</td>
<td>1M</td>
<td>8</td>
<td>Instruction</td>
<td>1</td>
<td>64</td>
<td>1</td>
<td>64</td>
</tr>
<tr>
<td>L2</td>
<td>512K</td>
<td>16M</td>
<td>8</td>
<td>Unified</td>
<td>2</td>
<td>1024</td>
<td>1</td>
<td>64</td>
</tr>
<tr>
<td>L3</td>
<td>16M</td>
<td>128M</td>
<td>16</td>
<td>Unified</td>
<td>3</td>
<td>16384</td>
<td>1</td>
<td>64</td>
</tr>
</tbody>
</table>

From numactl --hardware:

WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 8 nodes (0-7)
node 0 cpus: 0 1 2 3 32 33 34 35
node 0 size: 257862 MB

(Continued on next page)
Platform Notes (Continued)

node 0 free: 257609 MB
node 1 cpus: 4 5 6 7 36 37 38 39
node 1 size: 258045 MB
node 1 free: 257780 MB
node 2 cpus: 8 9 10 11 40 41 42 43
node 2 size: 258045 MB
node 2 free: 257835 MB
node 3 cpus: 12 13 14 15 44 45 46 47
node 3 size: 245936 MB
node 3 free: 245731 MB
node 4 cpus: 16 17 18 19 48 49 50 51
node 4 size: 258045 MB
node 4 free: 257467 MB
node 5 cpus: 20 21 22 23 52 53 54 55
node 5 size: 258011 MB
node 5 free: 257753 MB
node 6 cpus: 24 25 26 27 56 57 58 59
node 6 size: 258045 MB
node 6 free: 257838 MB
node 7 cpus: 28 29 30 31 60 61 62 63
node 7 size: 258043 MB
node 7 free: 257777 MB
node distances:

node 0   1   2   3   4   5   6   7
0:  10  11  11  11  32  32  32  32
1:  11  10  11  11  32  32  32  32
2:  11  11  10  11  32  32  32  32
3:  11  11  11  10  32  32  32  32
4:  32  32  32  32  10  11  11  11
5:  32  32  32  32  11  10  11  11
6:  32  32  32  32  11  11  10  11
7:  32  32  32  32  11  11  11  10

From /proc/meminfo
MemTotal:       2101286224 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP3"
    VERSION_ID="15.3"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"

(Continued on next page)
Cisco Systems  
Cisco UCS C245 M6 (AMD EPYC 7282 16-core) Processor

SPEC CPU®2017 Integer Rate Result

SPECrate®2017_int_base = 219
SPECrate®2017_int_peak = 240

CPU2017 License: 9019  
Test Date: Oct-2022
Test Sponsor: Cisco Systems  
 Hardware Availability: Aug-2021
Tested by: Cisco Systems  
Software Availability: Dec-2021

Platform Notes (Continued)

ID="sles"  
ID_LIKE="suse"  
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:15:sp3"

uname -a:  
Linux SPEC-SRV02 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9)  
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected  
CVE-2018-3620 (L1 Terminal Fault): Not affected  
Microarchitectural Data Sampling: Not affected  
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Full AMD retpoline, IBPB: conditional, IBRS_FW, STIBP: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Oct 24 05:50:

SPEC is set to: /home/cpu2017  
Filesystem Type Size Used Avail Use% Mounted on  
/dev/sda1 xfs 223G 10G 213G 5% /

From /sys/devices/virtual/dmi/id  
Vendor: Cisco Systems Inc
Product: UCSC-C245-M6SX
Serial: WZP251302NJ

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
16x 0xCE00 M386AAG40AM3-CWE 128 GB 4 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.

(Continued on next page)
Cisco UCS C245 M6 (AMD EPYC 7282 16-core Processor)

SPECrater®2017_int_base = 219
SPECrater®2017_int_peak = 240

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Oct-2022
CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Hardware Availability: Aug-2021
Software Availability: Dec-2021

Platform Notes (Continued)

BIOS Version: C245M6.4.2.2b.0.0509222122
BIOS Date: 05/09/2022
BIOS Revision: 5.14

(End of data from sysinfo program)

Compiler Version Notes

C | 502.gcc_r(peak)

AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base, peak)

AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

C | 502.gcc_r(peak)

AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base, peak)

AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: x86_64-unknown-linux-gnu

(Continued on next page)
Cisco Systems (Cisco UCS C245 M6 (AMD EPYC 7282 16-core Processor))

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Codec: 

<table>
<thead>
<tr>
<th>Compiler Version Notes (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thread model: posix</td>
</tr>
<tr>
<td>InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin</td>
</tr>
</tbody>
</table>

---

C++ | 523.xalancbmk_r (peak)

AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

---

C++ | 520.omnetpp_r (base, peak) 523.xalancbmk_r (base) 531.deepsjeng_r (base, peak) 541.leela_r (base, peak)

AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

---

C++ | 523.xalancbmk_r (peak)

AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

---

C++ | 520.omnetpp_r (base, peak) 523.xalancbmk_r (base) 531.deepsjeng_r (base, peak) 541.leela_r (base, peak)

AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

---

Test Date: Oct-2022
Hardware Availability: Aug-2021
Software Availability: Dec-2021

(Continued on next page)
Cisco Systems  
Cisco UCS C245 M6 (AMD EPYC 7282 16-core) Processor

| SPECrate®2017_int_base = 219 |
| SPECrate®2017_int_peak = 240 |

| CPU2017 License: 9019 | Test Date: Oct-2022 |
| Test Sponsor: Cisco Systems | Hardware Availability: Aug-2021 |
| Tested by: Cisco Systems | Software Availability: Dec-2021 |

**Compiler Version Notes (Continued)**

Fortran | 548.exchange2_r(base, peak)

---------------------------------------------
AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

**Base Compiler Invocation**

C benchmarks:
clang

C++ benchmarks:
clang++

Fortran benchmarks:
flang

**Base Portability Flags**

500.perlbench_r: -DSPEC_LINUX_X64 -DSPEC_LP64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:
-m64 -Wl,-allow-multiple-definition -Wl,-mllvm -Wl,-enable-licm-vrp
-fflto -Wl,-mllvm -Wl,-region-vectorize
-Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3

(Continued on next page)
Cisco Systems
Cisco UCS C245 M6 (AMD EPYC 7282 16-core Processor)  

**SPEC CPU®2017 Integer Rate Result**

Copyright 2017-2022 Standard Performance Evaluation Corporation

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_base</td>
<td>219</td>
</tr>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>240</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Test Date: Oct-2022  
Hardware Availability: Aug-2021  
Tested by: Cisco Systems  
Software Availability: Dec-2021

### Base Optimization Flags (Continued)

**C benchmarks (continued):**
- `-Wl,-mlirm -Wl,-enable-loop-fusion -O3 -march=znver3 -fveclib=AMDLIBM`
- `-ffast-math -fsstruct-layout=5 -mlirm -unroll-threshold=50`
- `-mlirm -inline-threshold=1000 -fremap-arrays`
- `-mlirm -function-specialize -fveclib=AMDLIBM`
- `-mlirm -enable-gvn-hoist -mlirm -global-vectorize-slp=true`
- `-mlirm -enable-licm-vrp -mlirm -reduce-array-computations=3`
- `-mlirm -enable-loop-fusion -z muldefs -ljamalibm -ljemalloc -lflang`

**C++ benchmarks:**
- `-m64 -std=c++98 -flto -Wl,-mlirm -Wl,-region-vectorize`
- `-Wl,-mlirm -Wl,-function-specialize`
- `-Wl,-mlirm -Wl,-align-all-nofallthru-blocks=6`
- `-Wl,-mlirm -Wl,-reduce-array-computations=3`
- `-Wl,-mlirm -Wl,-enable-loop-fusion -O3 -march=znver3 -fveclib=AMDLIBM`
- `-ffast-math -mlirm -enable-partial-unswitch`
- `-mlirm -unroll-threshold=100 -finline-aggressive`
- `-flv-function-specialization -mlirm -loop-unswitch-threshold=200000`
- `-mlirm -reroil-loops -mlirm -aggressive-loop-unswitch`
- `-mlirm -extra-vectorizer-passes -mlirm -reduce-array-computations=3`
- `-mlirm -global-vectorize-slp=true -mlirm -convert-pow-exp-to-int=false`
- `-mlirm -enable-loop-fusion -z muldefs -fvirtual-function-elimination`
- `-fvisibility=hidden -ljamalibm -ljemalloc -lflang`

**Fortran benchmarks:**
- `-m64 -Wl,-mlirm -Wl,-inline-recursion=4`
- `-Wl,-mlirm -Wl,-lsr-in-nested-loop -Wl,-mlirm -Wl,-enable-iv-split`
- `-flto -Wl,-mlirm -Wl,-region-vectorize`
- `-Wl,-mlirm -Wl,-function-specialize`
- `-Wl,-mlirm -Wl,-align-all-nofallthru-blocks=6`
- `-Wl,-mlirm -Wl,-reduce-array-computations=3`
- `-Wl,-mlirm -Wl,-enable-loop-fusion -O3 -march=znver3 -fveclib=AMDLIBM`
- `-ffast-math -z muldefs -mlirm -unroll-aggressive`
- `-mlirm -unroll-threshold=500 -ljamalibm -ljemalloc -lflang`

### Base Other Flags

**C benchmarks:**
- `-Wno-unused-command-line-argument`

**C++ benchmarks:**
- `-Wno-unused-command-line-argument`
Cisco Systems
Cisco UCS C245 M6 (AMD EPYC 7282 16-core)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2022 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C245 M6 (AMD EPYC 7282 16-core)

SPECrate®2017_int_base = 219
SPECrate®2017_int_peak = 240

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2022
Hardware Availability: Aug-2021
Software Availability: Dec-2021

Peak Compiler Invocation

C benchmarks:
clang

C++ benchmarks:
clang++

Fortran benchmarks:
flang

Peak Portability Flags

500.perlbench_r: -DSPEC_LINUX_X64 -DSPEC_LP64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: basepeak = yes

502.gcc_r: -m32 -Wl, -allow-multiple-definition
-Wl, -mllvm -Wl, -enable-licm-vrp -flto
-Wl, -mllvm -Wl, -function-specialize -Ofast -march=znver3
-fveclib=AMDLIBM -ffast-math -fstruct-layout=7
-mllvm -unroll-threshold=50 -fremap-arrays
-flv-function-specialization -mllvm -inline-threshold=1000
-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true
-mllvm -function-specialize -mllvm -enable-licm-vrp
-mllvm -reduce-array-computations=3 -fgnu89-inline
-ljemalloc

505.mcf_r: -m64 -Wl, -allow-multiple-definition
-Wl, -mllvm -Wl, -enable-licm-vrp -flto
-Wl, -mllvm -Wl, -function-specialize

(Continued on next page)
Cisco Systems
Cisco UCS C245 M6 (AMD EPYC 7282 16-core)
Processor

SPECrate®2017_int_base = 219
SPECrate®2017_int_peak = 240

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Oct-2022
Hardware Availability: Aug-2021
Software Availability: Dec-2021

Peak Optimization Flags (Continued)

505.mcf_r (continued):
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -ffast-math
-fstruct-layout=7 -mllvm -unroll-threshold=50
-fremap-arrays -flv-function-specialization
-mllvm -inline-threshold=1000 -mllvm -enable-gvn-hoist
-mllvm -global-vectorize-slp=true
-mllvm -function-specialize -mllvm -enable-lcm-vrp
-mllvm -reduce-array-computations=3 -lamdlibm -ljemalloc

525.x264_r: basepeak = yes
557.xz_r: basepeak = yes

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: -m32 -Wl,-mllvm -Wl,-do-block-reorder=aggressive -flto
-Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -ffast-math
-finline-aggressive -mllvm -unroll-threshold=100
-flv-function-specialization -mllvm -enable-lcm-vrp
-mllvm -reroll-loops -mllvm -aggressive-loop-unswitch
-mllvm -reduce-array-computations=3
-mllvm -global-vectorize-slp=true
-mllvm -do-block-reorder=aggressive
-fvirtual-function-elimination -fvisibility=hidden
-ljemalloc

531.deepsjeng_r: -m64 -std=c++98 -flto -Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -ffast-math
-finline-aggressive -mllvm -unroll-threshold=100
-flv-function-specialization -mllvm -enable-lcm-vrp
-mllvm -reroll-loops -mllvm -aggressive-loop-unswitch
-mllvm -reduce-array-computations=3
-mllvm -global-vectorize-slp=true
-fvirtual-function-elimination -fvisibility=hidden
-ljemalloc

(Continued on next page)
Cisco Systems
Cisco UCS C245 M6 (AMD EPYC 7282 16-core Processor)

SPECrate®2017_int_base = 219
SPECrate®2017_int_peak = 240

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2022
Hardware Availability: Aug-2021
Software Availability: Dec-2021

Peak Optimization Flags (Continued)

541.leela_r: Same as 531.deepsjeng_r

Fortran benchmarks:
-m64 -Wl,-mllvm -Wl,-inline-recursion=4
-Wl,-mllvm -Wl,-isr-in-nested-loop -Wl,-mllvm -Wl,-enable-iv-split
-fto -Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -03 -march=znver3
-fveclib=AMDLIBM -ffast-math -mllvm -unroll-aggressive
-mllvm -unroll-threshold=500 -lamdlibm -ljemalloc -lflang

Peak Other Flags

C benchmarks (except as noted below):
-Wno-unused-command-line-argument

502.gcc_r -L/usr/lib -Wno-unused-command-line-argument
-L/sppo/bin/cpu2017v118-aocc3-milanX/amd_rate_aocc320_milanx_A_lib/lib32

C++ benchmarks (except as noted below):
-Wno-unused-command-line-argument

523.xalancbmk_r -L/usr/lib -Wno-unused-command-line-argument
-L/sppo/bin/cpu2017v118-aocc3-milanX/amd_rate_aocc320_milanx_A_lib/lib32

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2022-10-24 08:51:38-0400.
Report generated on 2022-12-08 18:59:05 by CPU2017 PDF formatter v6442.
Originally published on 2022-12-08.