**Lenovo Global Technology**

**ThinkSystem SR645 V3**

*2.90 GHz, AMD EPYC 9254*

---

**CPU2017 License:** 9017  
**Test Sponsor:** Lenovo Global Technology  
**Tested by:** Lenovo Global Technology

**Test Date:** Dec-2022  
**Hardware Availability:** Feb-2023  
**Software Availability:** Nov-2022

---

**Copies**

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base (581)</th>
<th>SPECrate®2017_int_peak (598)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>96</td>
<td>407</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>96</td>
<td>494</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>96</td>
<td>586</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>96</td>
<td>293</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>96</td>
<td>297</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>96</td>
<td>746</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>96</td>
<td>844</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>96</td>
<td>846</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>96</td>
<td>1400</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>96</td>
<td>1360</td>
</tr>
</tbody>
</table>

---

**CPU Name:** AMD EPYC 9254  
**Max MHz:** 4150  
**Nominal:** 2900  
**Enabled:** 48 cores, 2 chips, 2 threads/core  
**Orderable:** 1.2 chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**Cache L2:** 1 MB I+D on chip per core  
**Cache L3:** 128 MB I+D on chip per chip, 32 MB shared / 6 cores  
**Other:** None  
**Memory:** 1536 GB (24 x 64 GB 2Rx4 PC5-4800B-P)  
**Storage:** 1 x 480 GB SATA SSD  
**Other:** None  

---

**OS:** SUSE Linux Enterprise Server 15 SP4 (x86_64)  
**Kernel:** 5.14.21-150400.22-default  
**Compiler:** C/C++/Fortran: Version 4.0.0 of AOCC  
**Parallel:** No  
**Firmware:** Lenovo BIOS Version KAE105F 1.20 released Dec-2022  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** 32/64-bit  
**Other:** None  

**Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
Lenovo Global Technology
ThinkSystem SR645 V3
(2.90 GHz, AMD EPYC 9254)

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>96</td>
<td>375</td>
<td>407</td>
<td>375</td>
<td>407</td>
<td>376</td>
<td>407</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>96</td>
<td>275</td>
<td>495</td>
<td>275</td>
<td>494</td>
<td>275</td>
<td>494</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>96</td>
<td>184</td>
<td>843</td>
<td>184</td>
<td>843</td>
<td>183</td>
<td>848</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>96</td>
<td>431</td>
<td>292</td>
<td>430</td>
<td>293</td>
<td>429</td>
<td>293</td>
</tr>
<tr>
<td>523.xalanbmk_r</td>
<td>96</td>
<td>136</td>
<td>743</td>
<td>136</td>
<td>746</td>
<td>132</td>
<td>767</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>96</td>
<td>120</td>
<td>1400</td>
<td>120</td>
<td>1400</td>
<td>120</td>
<td>1400</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>96</td>
<td>231</td>
<td>477</td>
<td>231</td>
<td>477</td>
<td>231</td>
<td>477</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>96</td>
<td>341</td>
<td>466</td>
<td>349</td>
<td>455</td>
<td>341</td>
<td>466</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>96</td>
<td>185</td>
<td>1360</td>
<td>185</td>
<td>1360</td>
<td>185</td>
<td>1360</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>96</td>
<td>372</td>
<td>279</td>
<td>371</td>
<td>279</td>
<td>371</td>
<td>279</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The AMD64 AOCC Compiler Suite is available at http://developer.amd.com/amd-aocc/

Submit Notes

The config file option 'submit' was used.
'numactl' was used to bind copies to the cores.
See the configuration file for details.

Operating System Notes

'ulimit -s unlimited' was used to set environment stack size limit
'ulimit -l 2097152' was used to set environment locked pages in memory limit

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

To limit dirty cache to 8% of memory, 'sysctl -w vm.dirty_ratio=8' run as root.
To limit swap usage to minimum necessary, 'sysctl -w vm.swappiness=1' run as root.
To free node-local memory and avoid remote memory usage,
'sysctl -w vm.zone_reclaim_mode=1' run as root.
To clear filesystem caches, 'sync; sysctl -w vm.drop_caches=3' run as root.
To disable address space layout randomization (ASLR) to reduce run-to-run variability,
'sysctl -w kernel.randomize_va_space=0' run as root.

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR645 V3
(2.90 GHz,AMD EPYC 9254)

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Operating System Notes (Continued)

```bash
echo 0 > /proc/sys/kernel/numa_balancing
To enable Transparent Hugepages (THP) only on request for base runs,
'echo madvise > /sys/kernel/mm/transparent_hugepage/enabled' run as root.
To enable THP for all allocations for peak runs,
'echo always > /sys/kernel/mm/transparent_hugepage/enabled' and
'echo always > /sys/kernel/mm/transparent_hugepage/defrag' run as root.
```

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
```
LD_LIBRARY_PATH =
"/home/cpu2017-1.1.8-amd-aocc400-genoa-B1b/amd_rate_aocc400_genoa_B_lib/
lib:/home/cpu2017-1.1.8-amd-aocc400-genoa-B1b/amd_rate_aocc400_genoa_B_l
ib/lib32:"
MALLOC_CONF = "retain:true"
```

Environment variables set by runcpu during the 523.xalancbmk_r peak run:
```
MALLOC_CONF = "thp:never"
```

General Notes

Binaries were compiled on a system with 2x AMD EPYC 9174F CPU + 1.5TiB Memory using RHEL 8.6

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS configuration:
Operating Mode set to Maximum Performance and then set it to Custom Mode
NUMA Nodes per Socket set to NPS4

Sysinfo program /home/cpu2017-1.1.8-amd-aocc400-genoa-B1b/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acacf64d
running on localhost Sat Dec 3 06:23:09 2022

SUT (System Under Test) info as seen by some common utilities.

(Continued on next page)
### Platform Notes (Continued)

For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

- model name: AMD EPYC 9254 24-Core Processor
- 2 "physical id"s (chips)
- 96 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores: 24
  - siblings: 48
  - physical 0: cores 0 1 2 3 4 5 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
  - physical 1: cores 0 1 2 3 4 5 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29

From lscpu from util-linux 2.37.2:

- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Address sizes: 52 bits physical, 57 bits virtual
- Byte Order: Little Endian
- CPU(s): 96
- On-line CPU(s) list: 0-95
- Vendor ID: AuthenticAMD
- Model name: AMD EPYC 9254 24-Core Processor
- CPU family: 25
- Model: 17
- Thread(s) per core: 2
- Core(s) per socket: 24
- Socket(s): 2
- Stepping: 1
- Frequency boost: enabled
- CPU max MHz: 4151.7568
- CPU min MHz: 1500.0000
- BogoMIPS: 5791.04
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush mmx fxsr sse sse2 ht syscall nx mmxext fxsr_opt pdelgb rdtscp lm constant_tsc rep_good nopl nonstop_tsc cpuid extd_apicid aperfmperf rafi pni pclmulqdq monitor ssse3 sse4_1 sse4_2 x2apic movbe popcnt aes avx f16c rdrand lahf_lm cmp_legacy svm extapic cr8_legacy abm sse4a misalignsse 3dnowprefetch osiw ibs skinit wdtt tce topoext perfctr_core perfctr_nb bext perfctr_llc mwaitx cpb cat_l3 cdp_l3 invpcid_single hw_pstate ssbd mba ibrs ibpb stibp vmcall fsgsbase bm1l avx2 smp bml2 ibrm invmce cqm rdt_a avx512f avx512qd rdseed adx smap avx512ifma clflushopt clwb avx512cd sha ni avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local avx512_bf16 clzero ierper xsaverpr rdpru wboinvd amd_ppin arat npt lbv svm_lock nrip_save tsc_scale vmcb_clean flushbyasid decodeasists pausefilter pfthreshold avic v_vmsave_vmload vgif v_spec_ctrl avx512vbmi umip pku ospe

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR645 V3
(2.90 GHz, AMD EPYC 9254)

**CPU2017 License:** 9017  
**Test Sponsor:** Lenovo Global Technology  
**Tested by:** Lenovo Global Technology

**Test Date:** Dec-2022  
**Hardware Availability:** Feb-2023  
**Software Availability:** Nov-2022

---

**SPEC CPU®2017 Integer Rate Result**

**SPECrate®2017_int_base = 581**  
**SPECrate®2017_int_peak = 598**

---

**Platform Notes (Continued)**

```
rpidid overflow_recov succor smca fsrm flush_l1d
Virtualization: AMD-V
L1d cache: 1.5 MiB (48 instances)
L1i cache: 1.5 MiB (48 instances)
L2 cache: 48 MiB (48 instances)
L3 cache: 256 MiB (8 instances)
NUMA node(s): 8
NUMA node0 CPU(s): 0-5,48-53
NUMA node1 CPU(s): 6-11,54-59
NUMA node2 CPU(s): 12-17,60-65
NUMA node3 CPU(s): 18-23,66-71
NUMA node4 CPU(s): 24-29,72-77
NUMA node5 CPU(s): 30-35,78-83
NUMA node6 CPU(s): 36-41,84-89
NUMA node7 CPU(s): 42-47,90-95
Vulnerability Itlb multihit: Not affected
Vulnerability L1tf: Not affected
Vulnerability Mds: Not affected
Vulnerability Meltdown: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitation
Vulnerability Spectre v2: Mitigation; Retpolines, IBPF conditional, IBRS_FW, STIBP always-on, RSB filling
Vulnerability Srbds: Not affected
Vulnerability Txz async abort: Not affected
```

From `lscpu --cache`:

```
NAME ONE-SIZE ALL-SIZE WAYS TYPE LEVEL SETS PHY-LINE COHERENCY-SIZE
L1d 32K 1.5M 8 Data 1 64 1 64
L1i 32K 1.5M 8 Instruction 1 64 1 64
L2 1M 48M 8 Unified 2 2048 1 64
L3 32M 256M 16 Unified 3 32768 1 64
```

/proc/cpuinfo cache data

```
cache size : 1024 KB
```

From `numactl --hardware`

```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 8 nodes (0-7)
node 0 cpus: 0 1 2 3 4 5 48 49 50 51 52 53
node 0 size: 193147 MB
node 0 free: 191924 MB
node 1 cpus: 6 7 8 9 10 11 54 55 56 57 58 59
node 1 size: 193519 MB
node 1 free: 193117 MB
```

(Continued on next page)
<table>
<thead>
<tr>
<th>Platform Notes (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>node 2 cpus: 12 13 14 15 16 17 60 61 62 63 64 65</td>
</tr>
<tr>
<td>node 2 free: 193118 MB</td>
</tr>
<tr>
<td>node 3 cpus: 18 19 20 21 22 23 66 67 68 69 70 71</td>
</tr>
<tr>
<td>node 3 size: 193519 MB</td>
</tr>
<tr>
<td>node 3 free: 193166 MB</td>
</tr>
<tr>
<td>node 4 cpus: 24 25 26 27 28 29 72 73 74 75 76 77</td>
</tr>
<tr>
<td>node 4 size: 193519 MB</td>
</tr>
<tr>
<td>node 4 free: 193225 MB</td>
</tr>
<tr>
<td>node 5 cpus: 30 31 32 33 34 35 78 79 80 81 82 83</td>
</tr>
<tr>
<td>node 5 size: 193519 MB</td>
</tr>
<tr>
<td>node 5 free: 193196 MB</td>
</tr>
<tr>
<td>node 6 cpus: 36 37 38 39 40 41 84 85 86 87 88 89</td>
</tr>
<tr>
<td>node 6 size: 193519 MB</td>
</tr>
<tr>
<td>node 6 free: 193167 MB</td>
</tr>
<tr>
<td>node 7 cpus: 42 43 44 45 46 47 90 91 92 93 94 95</td>
</tr>
<tr>
<td>node 7 size: 193325 MB</td>
</tr>
<tr>
<td>node 7 free: 193023 MB</td>
</tr>
<tr>
<td>node 0 1 2 3 4 5 6 7</td>
</tr>
</tbody>
</table>
| node distances:
0: 10 12 12 12 32 32 32 32 |
| 1: 12 10 12 12 32 32 32 32 |
| 2: 12 12 10 12 32 32 32 32 |
| 3: 12 12 12 10 32 32 32 32 |
| 4: 32 32 32 32 10 12 12 12 |
| 5: 32 32 32 32 10 12 12 12 |
| 6: 32 32 32 32 12 10 12 12 |
| 7: 32 32 32 32 12 12 10 12 |

From /proc/meminfo
MemTotal: 1584699796 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
   NAME="SLES"
   VERSION="15-SP4"
   VERSION_ID="15.4"
   PRETTY_NAME="SUSE Linux Enterprise Server 15 SP4"
   ID="sles"
   ID_LIKE="suse"
   ANSI_COLOR="0;32"
   CPE_NAME="cpe:/o:suse:sles:15:sp4"

(Continued on next page)
Platform Notes (Continued)

uname -a:
   Linux localhost 5.14.21-150400.22-default #1 SMP PREEMPT_DYNAMIC Wed May 11 06:57:18
   UTC 2022 (49db222) x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Retpolines, IBPB: conditional, IBRS_FW, STIBP: always-on, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Dec 3 06:18

SPEC is set to: /home/cpu2017-1.1.8-amd-aocc400-genoa-B1b
   Filesystem     Type Size Used Avail Use% Mounted on
   /dev/sdb3      xfs  442G   23G  419G   6% /

From /sys/devices/virtual/dmi/id
   Vendor: Lenovo
   Product: ThinkSystem SR645 V3 MB,Genoa,DDR5,Oahu,1U
   Product Family: ThinkSystem
   Serial: 1234567890

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   Memory:
      1x SK Hynix HMCG94AEBQA109N 64 GB 2 rank 4800
      23x SK Hynix HMCG94AEBQA123N 64 GB 2 rank 4800

   BIOS:
      BIOS Vendor: Lenovo
      BIOS Version: KAE105F-1.20
      BIOS Date: 12/01/2022
Lenovo Global Technology
ThinkSystem SR645 V3
(2.90 GHz, AMD EPYC 9254)

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

SPECrate®2017_int_base = 581
SPECrate®2017_int_peak = 598

Test Date: Dec-2022
Hardware Availability: Feb-2023
Software Availability: Nov-2022

BIOS Revision: 1.20
Firmware Revision: 1.20

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C     | 502.gcc_r(peak)
------------------------------------------------------------------------------
AMD clang version 14.0.6 (CLANG: AOCC_4.0.0-Build#389 2022_10_07) (based on
LLVM Mirror.Version.14.0.6)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc/aocc-compiler-rel-4.0-3206-389/bin

------------------------------------------------------------------------------
C     | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
     | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
AMD clang version 14.0.6 (CLANG: AOCC_4.0.0-Build#389 2022_10_07) (based on
LLVM Mirror.Version.14.0.6)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc/aocc-compiler-rel-4.0-3206-389/bin

------------------------------------------------------------------------------
C     | 502.gcc_r(peak)
------------------------------------------------------------------------------
AMD clang version 14.0.6 (CLANG: AOCC_4.0.0-Build#389 2022_10_07) (based on
LLVM Mirror.Version.14.0.6)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc/aocc-compiler-rel-4.0-3206-389/bin

------------------------------------------------------------------------------
C     | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
     | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
AMD clang version 14.0.6 (CLANG: AOCC_4.0.0-Build#389 2022_10_07) (based on
LLVM Mirror.Version.14.0.6)
Target: x86_64-unknown-linux-gnu
Thread model: posix

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR645 V3
(2.90 GHz, AMD EPYC 9254)

Compiler Version Notes (Continued)

InstalledDir: /opt/AMD/aocc/aocc-compiler-rel-4.0-3206-389/bin

==============================================================================
C++     | 523.xalancbmk_r(peak)
AMD clang version 14.0.6 (CLANG: AOCC_4.0.0-Build#389 2022_10_07) (based on LLVM Mirror.Version.14.0.6)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc/aocc-compiler-rel-4.0-3206-389/bin

==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
AMD clang version 14.0.6 (CLANG: AOCC_4.0.0-Build#389 2022_10_07) (based on LLVM Mirror.Version.14.0.6)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc/aocc-compiler-rel-4.0-3206-389/bin

==============================================================================
C++     | 523.xalancbmk_r(peak)
AMD clang version 14.0.6 (CLANG: AOCC_4.0.0-Build#389 2022_10_07) (based on LLVM Mirror.Version.14.0.6)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc/aocc-compiler-rel-4.0-3206-389/bin

==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
AMD clang version 14.0.6 (CLANG: AOCC_4.0.0-Build#389 2022_10_07) (based on LLVM Mirror.Version.14.0.6)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc/aocc-compiler-rel-4.0-3206-389/bin

==============================================================================
Fortran | 548.exchange2_r(base, peak)
(Continued on next page)
Lenovo Global Technology
ThinkSystem SR645 V3
(2.90 GHz, AMD EPYC 9254)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2023 Standard Performance Evaluation Corporation

Lenovo Global Technology
Test Date: Dec-2022
Test Sponsor: Lenovo Global Technology
CPU2017 License: 9017
Tested by: Lenovo Global Technology
Test Date: Dec-2022
Hardware Availability: Feb-2023
Software Availability: Nov-2022

SPECrater®2017_int_base = 581
SPECrater®2017_int_peak = 598

Compiler Version Notes (Continued)
AMD clang version 14.0.6 (CLANG: AOCC_4.0.0-Build#389 2022_10_07) (based on LLVM Mirror.Version.14.0.6)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc/aocc-compiler-rel-4.0-3206-389/bin

Base Compiler Invocation
C benchmarks:
clang
C++ benchmarks:
clang++
Fortran benchmarks:
flang

Base Portability Flags
500.perlbanch_r: -DSPEC_LINUX_X64 -DSPEC_LP64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-m64 -flto -Wl,-ml1vm -Wl,-align-all-nofallthru-blocks=6
-Wl,-ml1vm -Wl,-reduce-array-computations=3
-Wl,-ml1vm -Wl,-ldist-scalar-expand -fenable-aggressive-gather
-z muldefs -O3 -march=znver4 -fveclib=AMDLIBM -ffast-math
-fstruct-layout=7 -ml1vm -unroll-threshold=50
-ml1vm -inline-threshold=1000 -fremap-arrays -fstrip-mining

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR645 V3
(2.90 GHz, AMD EPYC 9254)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2023 Standard Performance Evaluation Corporation

Lenovo Global Technology

SPECRate®2017_int_base = 581
SPECRate®2017_int_peak = 598

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Test Date: Dec-2022
Tested by: Lenovo Global Technology
Hardware Availability: Feb-2023
Software Availability: Nov-2022

Base Optimization Flags (Continued)

C benchmarks (continued):
-mllvm -reduce-array-computations=3 -zopt -lamdlibm -lflang
-lamdalloc

C++ benchmarks:
-m64 -flto -W1, -mllvm -W1, -align-all-nofallthru-blocks=6
-W1, -mllvm -W1, -reduce-array-computations=3 -z muldefs -O3
-march=znver4 -fveclib=AMDLIBM -ffast-math
-mllvm -unroll-threshold=100 -finline-aggressive
-mllvm -loop-unswitch-threshold=200000
-mllvm -reduce-array-computations=3 -zopt
-fvirtual-function-elimination -fvisibility=hidden -lamdlibm -lflang
-lamdalloc-ext

Fortran benchmarks:
-m64 -flto -W1, -mllvm -W1, -align-all-nofallthru-blocks=6
-W1, -mllvm -W1, -reduce-array-computations=3
-W1, -mllvm -W1, -inline-recursion=4 -W1, -mllvm -W1, -lsr-in-nested-loop
-W1, -mllvm -W1, -enable-iv-split -z muldefs -O3 -march=znver4
-fveclib=AMDLIBM -ffast-math -fepilog-vectorization-of-inductions
-mllvm -optimize-strided-mem-cost -floop-transform
-mllvm -unroll-aggressive -mllvm -unroll-threshold=500 -lamdlibm
-lflang -lmdalloc

Base Other Flags

C benchmarks:
-Wno-unused-command-line-argument

C++ benchmarks:
-Wno-unused-command-line-argument

Fortran benchmarks:
-Wno-unused-command-line-argument

Peak Compiler Invocation

C benchmarks:
clang

C++ benchmarks:
clang++

(Continued on next page)
Peak Compiler Invocation (Continued)

Fortran benchmarks:
flang

Peak Portability Flags

500.perlbench_r: -DSPEC_LINUX_X64 -DSPEC_LP64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: basepeak = yes

502.gcc_r: -m32 -flto -z muldefs -Ofast -march=znver4
-ffast-math -fstruct-layout=7
-mllvm -unroll-threshold=50 -fremap-arrays -fstrip-mining
-mllvm -inline-threshold=1000
-mllvm -reduce-array-computations=3 -zopt -fgnu89-inline
-clang

505.mcf_r: -m64 -flto -Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver4 -ffast-math
-fstruct-layout=7 -mllvm -unroll-threshold=50
-fremap-arrays -fstrip-mining
-mllvm -inline-threshold=1000
-mllvm -reduce-array-computations=3 -zopt -lamdllib
-llflang -lamdalloc

525.x264_r: basepeak = yes
## Lenovo Global Technology

### ThinkSystem SR645 V3 (2.90 GHz, AMD EPYC 9254)

### SPEC CPU®2017 Integer Rate Result

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Lenovo Global Technology</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Lenovo Global Technology</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2022</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Feb-2023</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Nov-2022</td>
</tr>
</tbody>
</table>

### SPECrate®2017_int_base = 581

### SPECrate®2017_int_peak = 598

### Peak Optimization Flags (Continued)

**557.xz_r:** Same as 505.mcf_r

**C++ benchmarks:**

```
520.omnetpp_r: -m64 -flto -Wl,-mlllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mlllvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver4 -fveclib=AMDLIBM -ffast-math
-finline-aggressive -mlllvm -unroll-threshold=100
-mlllvm -reduce-array-computations=3 -zopt
-fvirtual-function-elimination -fvisibility=hidden
-lamdlibm -lamdalloc-ext
```

```
523.xalancbmk_r: -m32 -flto -Wl,-mlllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mlllvm -Wl,-reduce-array-computations=3
-Wl,-mlllvm -Wl,-do-block-reorder=aggressive
-fno-loop-reroll -Ofast -march=znver4 -fveclib=AMDLIBM
-ffast-math -finline-aggressive
-mlllvm -unroll-threshold=100
-mlllvm -reduce-array-computations=3 -zopt
-mlllvm -do-block-reorder=aggressive
-fvirtual-function-elimination -fvisibility=hidden
-lamdalloc-ext
```

```
531.deepsjeng_r: -m64 -flto -Wl,-mlllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mlllvm -Wl,-reduce-array-computations=3 -O3
-march=znver4 -fveclib=AMDLIBM -ffast-math
-mlllvm -unroll-threshold=100 -finline-aggressive
-mlllvm -loop-unswitch-threshold=200000
-mlllvm -reduce-array-computations=3 -zopt
-fvirtual-function-elimination -fvisibility=hidden
-lamdlibm -lamdalloc-ext
```

541.leela_r: basepeak = yes

**Fortran benchmarks:**

```
548.exchange2_r: basepeak = yes
```

### Peak Other Flags

C benchmarks (except as noted below):

```
-Wno-unused-command-line-argument
```

(Continued on next page)
## Lenovo Global Technology

ThinkSystem SR645 V3  
(2.90 GHz, AMD EPYC 9254)  

<table>
<thead>
<tr>
<th>SPEC CPU®2017 Integer Rate Result</th>
<th>Lenovo Global Technology</th>
<th>Test Date: Dec-2022</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_base = 581</td>
<td>Lenovo Global Technology</td>
<td>Hardware Availability: Feb-2023</td>
</tr>
<tr>
<td>SPECrate®2017_int_peak = 598</td>
<td>Lenovo Global Technology</td>
<td>Software Availability: Nov-2022</td>
</tr>
</tbody>
</table>

### Peak Other Flags (Continued)

502.gcc_r: -L/usr/lib32 -Wno-unused-command-line-argument  
-L/home/work/cpu2017/v118/aocc4/b1/rate/amd_rate_aocc400_genoa_B_lib/lib32

C++ benchmarks (except as noted below):  
-Wno-unused-command-line-argument

523.xalancbmk_r: -L/usr/lib32 -Wno-unused-command-line-argument  
-L/home/work/cpu2017/v118/aocc4/b1/rate/amd_rate_aocc400_genoa_B_lib/lib32

Fortran benchmarks:  
-Wno-unused-command-line-argument

The flags files that were used to format this result can be browsed at  
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-Genoa-O.html  
http://www.spec.org/cpu2017/flags/aocc400-flags.html

You can also download the XML flags sources by saving the following links:  
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-Genoa-O.xml  
http://www.spec.org/cpu2017/flags/aocc400-flags.xml

---

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2022-12-02 17:23:09-0500.  
Report generated on 2023-01-05 15:40:30 by CPU2017 PDF formatter v6442.  
Originally published on 2023-01-05.