## SPEC CPU®2017 Floating Point Rate Result

### Supermicro

**SuperServer SYS-121H-TNR**  
(X13DEM, Intel Xeon Gold 6418H)

<table>
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<th>CPU2017 License</th>
<th>001176</th>
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<td>Test Sponsor</td>
<td>Supermicro</td>
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<td>Tested by</td>
<td>Supermicro</td>
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<td>Hardware Availability</td>
<td>Jan-2023</td>
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<td>Software Availability</td>
<td>Jun-2022</td>
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### Hardware

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<th>508.namd_r</th>
<th>510.parest_r</th>
<th>511.povray_r</th>
<th>519.lbm_r</th>
<th>521.wrf_r</th>
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<th>527.cam4_r</th>
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### Software

- **OS**: SUSE Linux Enterprise Server 15 SP4  
  Kernel 5.14.21-150400.22-default
- **Compiler**: C/C++: Version 2022.1 of Intel oneAPI DPC++/C++ Compiler for Linux;  
  Fortran: Version 2022.1 of Intel Fortran Compiler for Linux;
- **Parallel**: No
- **Firmware**: No  
  Version 1.0a released Nov-2022
- **File System**: xfs
- **System State**: Run level 3 (multi-user)
- **Base Pointers**: 64-bit
- **Peak Pointers**: 64-bit
- **Other**: Jemalloc memory allocator V5.0.1
- **Power Management**: BIOS and OS set to prefer performance at the cost of additional power usage.

### CPU Name
- Intel Xeon Gold 6418H
- Max MHz: 4000
- Nominal: 2100
- Enabled: 48 cores, 2 chips, 2 threads/core
- Orderable: 2 chips
- Cache L1: 32 KB I + 48 KB D on chip per core
- L2: 2 MB I+D on chip per core
- L3: 60 MB I+D on chip per chip
- Other: None
- Memory: 2 TB (32 x 64 GB 2Rx4 PC5-4800B-R, running at 4400)
- Storage: 1 x 960 GB SATA III SSD
- Other: None
## Results Table

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</table>

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

**General Notes**

Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM memory using Red Hat Enterprise Linux 8.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
General Notes (Continued)

sync; echo 3>       /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Power Technology = Custom
Power Performance Tuning = BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode = Performance
DCU Streamer Prefetcher = Disable
SNC = Enable SNC2 (2-clusters)
LLC Dead Line Alloc = Disable
KTI Prefetch = Enable
Stale AtoS = Disable
Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on localhost Thu Nov 24 20:05:51 2022

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6418H
2 "physical id"s (chips)
96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
Supermicro
SuperServer SYS-121H-TNR
(X13DEM, Intel Xeon Gold 6418H)

CPU2017 License: 001176
Test Sponsor: Supermicro
Tested by: Supermicro

Test Date: Nov-2022
Hardware Availability: Jan-2023
Software Availability: Jun-2022

Platform Notes (Continued)

From lscpu from util-linux 2.37.2:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Address sizes: 46 bits physical, 57 bits virtual
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Vendor ID: GenuineIntel
Model name: Intel(R) Xeon(R) Gold 6418H
CPU family: 6
Model: 143
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
Stepping: 8
Frequency boost: enabled
CPU max MHz: 2101.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdcache rdtrace lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault ebpx_cat_13 cat_12 cat_11 cat_10 cat_9 cat_8 cat_7 cat_6 cat_5 cat_4 cat_3 cat_2 cat_1 cat_0
invcache_single icache_single dcache_single
L1d cache: 2.3 MiB (48 instances)
L1i cache: 1.5 MiB (48 instances)
L2 cache: 96 MiB (48 instances)
L3 cache: 120 MiB (2 instances)
NUMA node(s): 4
NUMA node0 CPU(s): 0-11,48-59
NUMA node1 CPU(s): 12-23,60-71
NUMA node2 CPU(s): 24-35,72-83
NUMA node3 CPU(s): 36-47,84-95
Vulnerability Itlb multihit: Not affected
Vulnerability L1ttl: Not affected

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

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SPECrater®2017_fp_peak = 513

CPU2017 License: 001176
Test Sponsor: Supermicro
Test Date: Nov-2022
Tested by: Supermicro
Software Availability: Jun-2022
Hardware Availability: Jan-2023

Platform Notes (Continued)

Vulnerability Mds: Not affected
Vulnerability Meltdown: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitization
Vulnerability Spectre v2: Mitigation; Enhanced IBRS, IBPB conditional, RSB filling
Vulnerability Srbds: Not affected
Vulnerability Tsx async abort: Not affected

From lscpu --cache:
NAME ONE-SIZE ALL-SIZE WAYS TYPE LEVEL SETS PHY-LINE COHERENCY-SIZE
L1d 48K 2.3M 12 Data 1 64 1 64
L1i 32K 1.5M 8 Instruction 1 64 1 64
L2 2M 96M 16 Unified 2 2048 1 64
L3 60M 120M 15 Unified 3 65536 1 64

/proc/cpuinfo cache data
    cache size : 61440 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
    available: 4 nodes (0-3)
    node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 60 61 62 63 64 65 66 67 68 69 70 71
    node 0 size: 515728 MB
    node 0 free: 500663 MB
    node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 60 61 62 63 64 65 66 67 68 69 70 71
    node 1 size: 516089 MB
    node 1 free: 505842 MB
    node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 72 73 74 75 76 77 78 79 80 81 82 83
    node 2 size: 516089 MB
    node 2 free: 505862 MB
    node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 84 85 86 87 88 89 90 91 92 93 94 95
    node 3 size: 516026 MB
    node 3 free: 505513 MB
    node distances:
    node 0 1 2 3
      0: 10 12 21 21
      1: 12 10 21 21
      2: 21 21 10 12
      3: 21 21 12 10

From /proc/meminfo
    MemTotal: 2113468612 kB
    HugePages_Total: 0
    Hugepagesize: 2048 kB

(Continued on next page)
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Tested by: Supermicro

Platform Notes (Continued)

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has ondemand

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP4"
    VERSION_ID="15.4"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP4"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp4"

uname -a:
  Linux localhost 5.14.21-150400.22-default #1 SMP PREEMPT_DYNAMIC Wed May 11 06:57:18 UTC 2022 (49db222) x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected
run-level 3 Nov 24 13:24
SPEC is set to: /home/cpu2017
  Filesystem  Type  Size  Used  Avail  Use% Mounted on
  /dev/sda2    xfs   892G  48G  844G   6%  /

From /sys/devices/virtual/dmi/id
  Vendor: Supermicro
  Product: Super Server
  Product Family: Family
  Serial: 0123456789

(Continued on next page)
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Platform Notes (Continued)

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
- 28x SK Hynix HMCG94MEBRA109N 64 GB 2 rank 4800, configured at 4400
- 4x SK Hynix HMCG94MEBRA124N 64 GB 2 rank 4800, configured at 4400

BIOS:
- BIOS Vendor: American Megatrends International, LLC.
- BIOS Version: 1.0a
- BIOS Date: 11/18/2022
- BIOS Revision: 5.29

(End of data from sysinfo program)

Compiler Version Notes

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<td>Copyright (C) 1985–2022 Intel Corporation. All rights reserved.</td>
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Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifx icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifx

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z, muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Peak Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifx

Benchmarks using both Fortran and C:
ifx icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifx
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<tr>
<th>Test Sponsor</th>
<th>Hardware Availability</th>
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<tr>
<td>Supermicro</td>
<td>Jan-2023</td>
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<th>Software Availability</th>
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<td>Supermicro</td>
<td>Jun-2022</td>
</tr>
</tbody>
</table>

#### Peak Portability Flags
Same as Base Portability Flags

#### Peak Optimization Flags

**C benchmarks:**

- **519.lbm_r:**
  - basepeak = yes

- **538.imagick_r:**
  - basepeak = yes

- **544.nab_r:**
  - -w  
  - -std=c11  
  - -m64  
  - -Wl,-z,muldefs  
  -xCORE-AVX512  
  - -Ofast  
  - -ffast-math  
  - -flto  
  - -mfpmath=sse  
  - -funroll-loops  
  - -qopt-mem-layout-trans=4  
  - -qopt-zmm-usage=high  
  - -ljemalloc  
  - -L/usr/local/jemalloc64-5.0.1/lib

**C++ benchmarks:**

- **508.namd_r:**
  - basepeak = yes

- **510.parest_r:**
  - -w  
  - -m64  
  - -Wl,-z,muldefs  
  -xCORE-AVX512  
  - -Ofast  
  - -ffast-math  
  - -flto  
  - -mfpmath=sse  
  - -funroll-loops  
  - -qopt-mem-layout-trans=4  
  - -L/usr/local/jemalloc64-5.0.1/lib

**Fortran benchmarks:**

- **503.bwaves_r:**
  - basepeak = yes

- **549.fotonik3d_r:**
  - basepeak = yes

- **554.roms_r:**
  - -w  
  - -m64  
  - -Wl,-z,muldefs  
  -xCORE-AVX512  
  - -Ofast  
  - -ffast-math  
  - -flto  
  - -mfpmath=sse  
  - -funroll-loops  
  - -qopt-mem-layout-trans=4  
  - -nostandard-realloc-lhs  
  - -align array32byte  
  - -auto  
  - -L/usr/local/jemalloc64-5.0.1/lib

**Benchmarks using both Fortran and C:**

- -w  
  - -std=c11  
  - -Wl,-z,muldefs  
  -xCORE-AVX512  
  - -Ofast  
  - -ffast-math  
  - -flto  
  - -mfpmath=sse  
  - -funroll-loops  
  - -qopt-mem-layout-trans=4  
  - -nostandard-realloc-lhs  
  - -align array32byte  
  - -auto  
  - -L/usr/local/jemalloc64-5.0.1/lib

**Benchmarks using both C and C++:**

(Continued on next page)
Supermicro
SuperServer SYS-121H-TNR
(X13DEM, Intel Xeon Gold 6418H)

SPECrate®2017_fp_base = 499
SPECrate®2017_fp_peak = 513

CPU2017 License: 001176
Test Sponsor: Supermicro
Test Date: Nov-2022
Tested by: Supermicro
Hardware Availability: Jan-2023
Software Availability: Jun-2022

Peak Optimization Flags (Continued)

511.povray_r: -w -m64 -std=c11 -Wl,-z,muldefs
                 -fprofile-generate(pass 1)
                 -fprofile-use=default.profdata(pass 2) -xCORE-AVX512
                 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops
                 -qopt-mem-layout-trans=4 -ljemalloc
                 -L/usr/local/jemalloc64-5.0.1/lib

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:
                 -w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
                 -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
                 -nostandard-realloc-lhs -align array32byte -auto -ljemalloc
                 -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Supermicro-Platform-Settings-V1.2-SPR-revC.xml

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