SPEC CPU®2017 Integer Rate Result

xFusion

xFusion 2288H V5 (Intel Xeon Silver 4210R)

SPECraté®2017_int_base = 135

SPECraté®2017_int_peak = Not Run

CPU2017 License: 6488
Test Sponsor: xFusion
Tested by: xFusion
Test Date: Jan-2023
Hardware Availability: Apr-2019
Software Availability: May-2022

Copies

<table>
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<th>500.perlbench_r</th>
<th>502.gcc_r</th>
<th>505.mcf_r</th>
<th>520.omnetpp_r</th>
<th>523.xalanchmk_r</th>
<th>525.x264_r</th>
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<th>541.leela_r</th>
<th>548.exchange2_r</th>
<th>557.xz_r</th>
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SPECrate®2017_int_base (135)

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</table>

xFusion 2288H V5 (Intel Xeon Silver 4210R)

Hardware

CPU Name: Intel Xeon Silver 4210R
Max MHz: 3200
Nominal: 2400
Enabled: 20 cores, 2 chips, 2 threads/core
Orderable: 1.2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 13.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)
Storage: 1 x 960 GB SATA SSD
Other: None

Software

OS: Red Hat Enterprise Linux release 8.4 (Ootpa) 4.18.0-305.el8.x86_64
Compiler: C/C++: Version 2022.1 of Intel oneAPI DPC++/C++ Compiler for Linux;
          Fortran: Version 2022.1 of Intel Fortran Compiler for Linux;
Parallel: No
Firmware: Version 8.37 Released Aug-2022
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
SPEC CPU®2017 Integer Rate Result

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xFusion 2288H V5 (Intel Xeon Silver 4210R)

CPU2017 License: 6488
Test Sponsor: xFusion
Tested by: xFusion

SPECCore®2017_int_base = 135
SPECCore®2017_int_peak = Not Run

Test Date: Jan-2023
Hardware Availability: Apr-2019
Software Availability: May-2022

Results Table

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Compiler Notes

SPEC has ruled that the compiler used for this result was performing a compilation that specifically improves the performance of the 523.xalancbmk_r / 623.xalancbmk_s benchmarks using a priori knowledge of the SPEC code and dataset to perform a transformation that has narrow applicability.

In order to encourage optimizations that have wide applicability (see rule 1.4
https://www.spec.org/cpu2017/Docs/runrules.html#rule_1.4), SPEC will no longer publish results using this optimization.

This result is left in the SPEC results database for historical reference.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/spec2017/lib/intel64:/spec2017/lib/ia32:/spec2017/je5.0.1-32"
MALLOC_CONF = "retain:true"
General Notes

Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM
memory using Red Hat Enterprise Linux 8.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

Platform Notes

BIOS configuration:
Power Policy Set to Performance
XPT Prefetch set to Enabled
Sysinfo program /spec2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf064d
running on localhost.localdomain Sat Jan 14 14:24:25 2023
SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
    2 "physical id"s (chips)
    40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu from util-linux 2.32.1:
    Architecture:        x86_64
    CPU op-mode(s):      32-bit, 64-bit
    Byte Order:          Little Endian
    CPU(s):              40
    On-line CPU(s) list: 0-39
    Thread(s) per core:  2
    Core(s) per socket: 10
    Socket(s):           2
    NUMA node(s):        2
    Vendor ID:           GenuineIntel
    BIOS Vendor ID:      Intel(R) Corporation
    CPU family:          6
    Model:               85
    Model name:          Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
    BIOS Model name:     Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
    Stepping:            7
    CPU MHz:             2900.076
    CPU max MHz:         3200.000

(Continued on next page)
Platform Notes (Continued)

CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9,20-29
NUMA node1 CPU(s): 10-19,30-39
Flags: fpu vme de pse mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfimerf pni pclmulqdq dtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm
pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c
rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat13 cdp13 invpcid_single sbbd
mbi ibrs ibpb stibp ibrs_enhanced tpr_shadow vmi flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bm1 hle avx2 smep bmi2 erms invpcid cmq mpx rdt_a avx512f
avx512dq rdseed adx smap cflushtype clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsave cqm l1c cqm_occup_l1c cqm_mbb_total cqm_mbb_local
dtherm ida arat pin pts pkup ospe avx512_vnni md_clear flush_l1d arch_capabilities

/proc/cpuinfo cache data
  cache size: 14080 KB

From /proc/meminfo
  MemTotal: 790809192 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/sbin/tuned-adm active
  Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release: NAME="Red Hat Enterprise Linux"
  VERSION="8.4 (Ootpa)"
  ID="rhel"
  ID_LIKE="fedora"
  VERSION_ID="8.4"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="Red Hat Enterprise Linux 8.4 (Ootpa)"
  ANSI_COLOR="0;31"
  redhat-release: Red Hat Enterprise Linux release 8.4 (Ootpa)
xFusion

xFusion 2288H V5 (Intel Xeon Silver 4210R)

spec

SPECCPU®2017 Integer Rate Result

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SPECCPU®2017_int_base = 135
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CPU2017 License: 6488
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Test Date: Jan-2023
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Platform Notes (Continued)

system-release: Red Hat Enterprise Linux release 8.4 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.4:ga

uname -a:
Linux localhost.localdomain 4.18.0-305.el8.x86_64 #1 SMP Thu Apr 29 08:54:30 EDT 2021
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store
CVE-2017-5763 (Speculative Store Bypass):
Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):
Mitigation: uservcopy/swaps barriers and __user pointer
sanitization
CVE-2017-5717 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB:
conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):
Mitigation: TSX disabled

run-level 3 Jan 14 12:32
SPEC is set to: /spec2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda4 xfs 859G 36G 824G 5% /

From /sys/devices/virtual/dmi/id
Vendor: XFUSION
Product: 2288H V5
Product Family: Purley
Serial: Serial

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
24x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

BIOS:
BIOS Vendor: XFUSION
BIOS Version: 8.37
BIOS Date: 08/25/2022
BIOS Revision: 8.37

(End of data from sysinfo program)

Compiler Version Notes

============================================================================================================
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) 525.x264_r(base) 557.xz_r(base)
------------------------------------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
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(Continued on next page)
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Compiler Version Notes (Continued)

C++ | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base) 541.leela_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

Fortran | 548.exchange2_r(base)

Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifx

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-ffto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4

(Continued on next page)
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Base Optimization Flags (Continued)

C benchmarks (continued):
-LL/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -gopt-mem-layout-trans=4
-LL/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -gopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-LL/usr/local/intel/compiler/2022.1.0/linux/compiler/lib/intel64_lin
-lqkmalloc

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/xFusion-Platform-Settings-CSL-V1.1.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/xFusion-Platform-Settings-CSL-V1.1.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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