# SPEC CPU®2017 Floating Point Rate Result

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## Dell Inc.

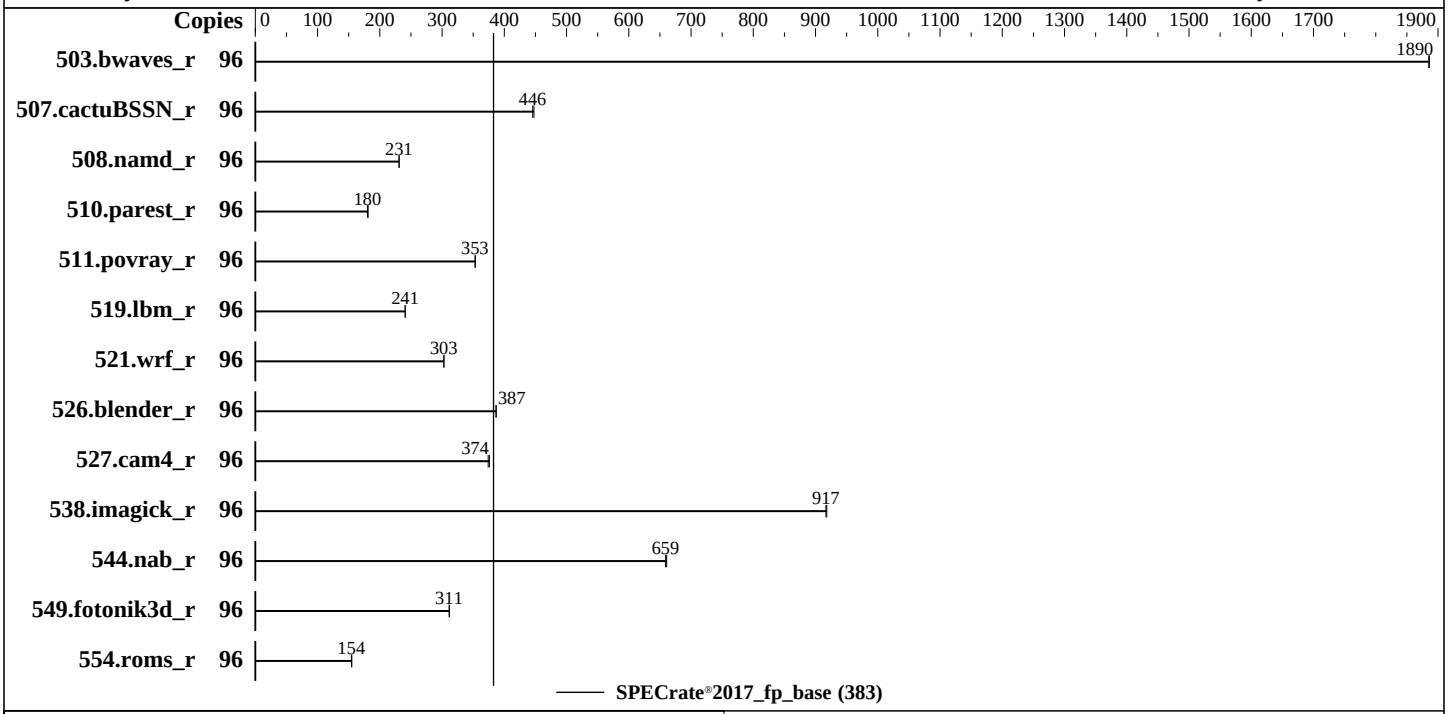
PowerEdge R750 (Intel Xeon Gold 5318Y, 2.10 GHz)

SPECrate®2017_fp_base = 383

SPECrate®2017_fp_peak = Not Run

**CPU2017 License:** 6573
**Test Sponsor:** Dell Inc.
**Tested by:** Dell Inc.

**Test Date:** Jan-2023
**Hardware Availability:** May-2021
**Software Availability:** Jun-2022




## Hardware

| | |
|---|---|
| CPU Name: | Intel Xeon Gold 5318Y |
| Max MHz: | 3400 |
| Nominal: | 2100 |
| Enabled: | 48 cores, 2 chips, 2 threads/core |
| Orderable: | 1,2 chips |
| Cache L1: | 32 KB I + 48 KB D on chip per core |
| L2: | 1.25 MB I+D on chip per core |
| L3: | 36 MB I+D on chip per chip |
| Other: | None |
| Memory: | 512 GB (16 x 32 GB 2Rx4 PC4-3200AA-R, running at 2933) |
| Storage: | 125 GB on tmpfs |
| Other: | None |

## Software

| | |
|---|---|
| OS: | SUSE Linux Enterprise Server 15 SP4 5.14.21-150400.22-default |
| Compiler: | C/C++: Version 2022.1 of Intel oneAPI DPC++/C++ Compiler for Linux; Fortran: Version 2022.1 of Intel Fortran Compiler for Linux; |
| Parallel: | No |
| Firmware: | Version 1.9.2 released Nov-2022 |
| File System: | tmpfs |
| System State: | Run level 5 (graphical multi-user) |
| Base Pointers: | 64-bit |
| Peak Pointers: | Not Applicable |
| Other: | jemalloc memory allocator V5.0.1 |
| Power Management: | BIOS and OS set to prefer performance at the cost of additional power usage. |

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## Results Table

| Benchmark | Base | | | | | | | Peak | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Copies | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio | Copies | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio |
| 503.bwaves_r | 96 | 510 | 1890 | **511** | **1890** | | | | | | | | | |
| 507.cactuBSSN_r | 96 | 272 | 448 | **273** | **446** | | | | | | | | | |
| 508.namd_r | 96 | 395 | 231 | **395** | **231** | | | | | | | | | |
| 510.parest_r | 96 | 1386 | 181 | **1394** | **180** | | | | | | | | | |
| 511.povray_r | 96 | 634 | 354 | **635** | **353** | | | | | | | | | |
| 519.lbm_r | 96 | **420** | **241** | 420 | 241 | | | | | | | | | |
| 521.wrf_r | 96 | **710** | **303** | 710 | 303 | | | | | | | | | |
| 526.blender_r | 96 | **378** | **387** | 378 | 387 | | | | | | | | | |
| 527.cam4_r | 96 | 446 | 376 | **449** | **374** | | | | | | | | | |
| 538.imagick_r | 96 | 260 | 918 | **260** | **917** | | | | | | | | | |
| 544.nab_r | 96 | 244 | 661 | **245** | **659** | | | | | | | | | |
| 549.fotonik3d_r | 96 | 1199 | 312 | **1202** | **311** | | | | | | | | | |
| 554.roms_r | 96 | 984 | 155 | **988** | **154** | | | | | | | | | |

**SPECrate®2017_fp_base = 383**

**SPECrate®2017_fp_peak = Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

```
The numactl mechanism was used to bind copies to processors. The config file option 'submit'
was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.
```

## Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
```

## Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
     "/mnt/ramdisk/cpu2017-1.1.8-ic2022.1/lib/intel64:/mnt/ramdisk/cpu2017-1.
     1.8-ic2022.1/je5.0.1-64"
MALLOC_CONF = "retain:true"
```

## General Notes

```
Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM
memory using Red Hat Enterprise Linux 8.4
Transparent Huge Pages enabled by default
```

**(Continued on next page)**

## General Notes (Continued)

```
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>       /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

Benchmark run from a 125 GB ramdisk created with the cmd: "mount -t tmpfs -o size=125G tmpfs /mnt/ramdisk"
```

## Platform Notes

```
BIOS settings:
        DIMM Self Healing on
    Uncorrectable Memory Error : Disabled
     Virtualization Technology : Disabled
               Sub NUMA Cluster : 2-way Clustering
       DCU Streamer Prefetcher : Disabled
                   LLC Prefetch : Disabled
           Dead Line LLC Alloc : Disabled
                Optimizer Mode : Enabled

                System Profile : Custom
          CPU Power Management : Maximum Performance
                           C1E : Disabled
                      C States : Autonomous
           Memory Patrol Scrub : Disabled
      Energy Efficiency Policy : Performance
            PCI ASPM L1 Link
              Power Management : Disabled

Sysinfo program /mnt/ramdisk/cpu2017-1.1.8-ic2022.1/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on localhost Thu Jan 12 22:04:11 2023

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
```

**(Continued on next page)**

## Platform Notes (Continued)

```
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

  From /proc/cpuinfo
     model name : Intel(R) Xeon(R) Gold 5318Y CPU @ 2.10GHz
        2  "physical id"s (chips)
        96 "processors"
     cores, siblings (Caution: counting these is hw and system dependent. The following
     excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
        cpu cores : 24
        siblings  : 48
        physical 0: cores 0 1 10 11 12 13 14 15 16 17 18 19 20 21 22 23
        physical 1: cores 0 1 10 11 12 13 14 15 16 17 18 19 20 21 22 23

  From lscpu from util-linux 2.37.2:
       Architecture:                    x86_64
       CPU op-mode(s):                  32-bit, 64-bit
       Address sizes:                   46 bits physical, 57 bits virtual
       Byte Order:                      Little Endian
       CPU(s):                          96
       On-line CPU(s) list:             0-95
       Vendor ID:                       GenuineIntel
       Model name:                      Intel(R) Xeon(R) Gold 5318Y CPU @ 2.10GHz
       CPU family:                      6
       Model:                           106
       Thread(s) per core:              2
       Core(s) per socket:              24
       Socket(s):                       2
       Stepping:                        6
       CPU max MHz:                     3400.0000
       CPU min MHz:                     800.0000
       BogoMIPS:                        4200.00
       Flags:                           fpu vme de pse tsc msr pae mce cx8 apic sep mtrr
       pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx
       pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology
       nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl smx est tm2 ssse3
       sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
       tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
       epb cat_l3 invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced fsgsbase
       tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq
       rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw
       avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
       cqm_mbm_local split_lock_detect wbnoinvd dtherm ida arat pln pts hwp hwp_act_window
       hwp_epp hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq
       avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid fsrm md_clear pconfig
       flush_l1d arch_capabilities
       L1d cache:                       2.3 MiB (48 instances)
       L1i cache:                       1.5 MiB (48 instances)
```

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## Platform Notes (Continued)

```
      L2 cache:                         60 MiB (48 instances)
      L3 cache:                         72 MiB (2 instances)
      NUMA node(s):                     4
      NUMA node0 CPU(s):
      0,4,8,12,16,20,24,28,32,36,40,44,48,52,56,60,64,68,72,76,80,84,88,92
      NUMA node1 CPU(s):
      2,6,10,14,18,22,26,30,34,38,42,46,50,54,58,62,66,70,74,78,82,86,90,94
      NUMA node2 CPU(s):
      1,5,9,13,17,21,25,29,33,37,41,45,49,53,57,61,65,69,73,77,81,85,89,93
      NUMA node3 CPU(s):
      3,7,11,15,19,23,27,31,35,39,43,47,51,55,59,63,67,71,75,79,83,87,91,95
      Vulnerability Itlb multihit:      Not affected
      Vulnerability L1tf:               Not affected
      Vulnerability Mds:                Not affected
      Vulnerability Meltdown:           Not affected
      Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via
      prctl and seccomp
      Vulnerability Spectre v1:         Mitigation; usercopy/swapgs barriers and __user
      pointer sanitization
      Vulnerability Spectre v2:         Mitigation; Enhanced IBRS, IBPB conditional, RSB
      filling
      Vulnerability Srbds:              Not affected
      Vulnerability Tsx async abort:    Not affected

  From lscpu --cache:
      NAME ONE-SIZE ALL-SIZE WAYS TYPE        LEVEL  SETS PHY-LINE COHERENCY-SIZE
      L1d       48K     2.3M   12 Data            1    64        1             64
      L1i       32K     1.5M    8 Instruction     1    64        1             64
      L2       1.3M      60M   20 Unified         2  1024        1             64
      L3        36M      72M   12 Unified         3 49152        1             64

  /proc/cpuinfo cache data
     cache size : 36864 KB

  From numactl --hardware
  WARNING: a numactl 'node' might or might not correspond to a physical chip.
    available: 4 nodes (0-3)
    node 0 cpus: 0 4 8 12 16 20 24 28 32 36 40 44 48 52 56 60 64 68 72 76 80 84 88 92
    node 0 size: 128410 MB
    node 0 free: 127434 MB
    node 1 cpus: 2 6 10 14 18 22 26 30 34 38 42 46 50 54 58 62 66 70 74 78 82 86 90 94
    node 1 size: 129017 MB
    node 1 free: 128341 MB
    node 2 cpus: 1 5 9 13 17 21 25 29 33 37 41 45 49 53 57 61 65 69 73 77 81 85 89 93
    node 2 size: 129017 MB
    node 2 free: 120932 MB
    node 3 cpus: 3 7 11 15 19 23 27 31 35 39 43 47 51 55 59 63 67 71 75 79 83 87 91 95
```

**(Continued on next page)**

## Platform Notes (Continued)

```
   node 3 size: 128954 MB
   node 3 free: 128186 MB
   node distances:
   node   0   1   2   3
     0:  10  11  20  20
     1:  11  10  20  20
     2:  20  20  10  11
     3:  20  20  11  10

 From /proc/meminfo
    MemTotal:       527770268 kB
    HugePages_Total:       0
    Hugepagesize:       2048 kB

 /sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
    performance

 From /etc/*release* /etc/*version*
    os-release:
       NAME="SLES"
       VERSION="15-SP4"
       VERSION_ID="15.4"
       PRETTY_NAME="SUSE Linux Enterprise Server 15 SP4"
       ID="sles"
       ID_LIKE="suse"
       ANSI_COLOR="0;32"
       CPE_NAME="cpe:/o:suse:sles:15:sp4"

 uname -a:
    Linux localhost 5.14.21-150400.22-default #1 SMP PREEMPT_DYNAMIC Wed May 11 06:57:18
    UTC 2022 (49db222) x86_64 x86_64 x86_64 GNU/Linux

 Kernel self-reported vulnerability status:

 CVE-2018-12207 (iTLB Multihit):                          Not affected
 CVE-2018-3620 (L1 Terminal Fault):                       Not affected
 Microarchitectural Data Sampling:                        Not affected
 CVE-2017-5754 (Meltdown):                                Not affected
 CVE-2018-3639 (Speculative Store Bypass):                Mitigation: Speculative Store
                                                          Bypass disabled via prctl and
                                                          seccomp
 CVE-2017-5753 (Spectre variant 1):                       Mitigation: usercopy/swapgs
                                                          barriers and __user pointer
                                                          sanitization
 CVE-2017-5715 (Spectre variant 2):                      Mitigation: Enhanced IBRS, IBPB:
                                                          conditional, RSB filling
 CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
```

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## Platform Notes (Continued)

```
 CVE-2019-11135 (TSX Asynchronous Abort):              Not affected

 run-level 5 Jan 12 18:55

 SPEC is set to: /mnt/ramdisk/cpu2017-1.1.8-ic2022.1
    Filesystem     Type   Size  Used Avail Use% Mounted on
    tmpfs          tmpfs  125G  3.6G  122G   3% /mnt/ramdisk

 From /sys/devices/virtual/dmi/id
     Vendor:         Dell Inc.
     Product:        PowerEdge R750
     Product Family: PowerEdge
     Serial:         3Z6GMH3

 Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
 interpret this section. The 'dmidecode' program reads system data which is "intended to
 allow hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   Memory:
     16x 00CE063200CE M393A4G43AB3-CWE 32 GB 2 rank 3200, configured at 2933

 BIOS:
    BIOS Vendor:       Dell Inc.
    BIOS Version:      1.9.2
    BIOS Date:         11/17/2022
    BIOS Revision:     1.9

 (End of data from sysinfo program)
```

## Compiler Version Notes

```
==============================================================================
C              | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++            | 508.namd_r(base) 510.parest_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
```

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## Compiler Version Notes (Continued)

```
==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version
  2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran         | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version
  2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
------------------------------------------------------------------------------
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------------------------------------------------------------------------------
```

## Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifx

Benchmarks using both Fortran and C:
ifx icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifx

## Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

## Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

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## Base Optimization Flags (Continued)

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic2022-official-linux64-revB.html
http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-Intel-Xeon-v1.3.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2022-official-linux64-revB.xml
http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-Intel-Xeon-v1.3.xml


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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