Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

### Hardware
- **CPU Name:** Intel Xeon Gold 6448Y
- **Max MHz:** 4100
- **Nominal:** 2100
- **Enabled:** 64 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **L2:** 2 MB I+D on chip per core
- **L3:** 60 MB I+D on chip per chip
- **Other:** None
- **Memory:** 1 TB (16 x 64 GB 2Rx4 PC5-4800B-R)
- **Storage:** 1 x 960 GB M.2 SSD SATA
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 15 SP4 5.14.21-150400.22-default
- **Compiler:** C/C++: Version 2023.0 of Intel oneAPI DPC++/C++ Compiler for Linux;
  Fortran: Version 2023.0 of Intel Fortran Compiler for Linux;
- **Parallel:** No
- **Firmware:** Version 4.2.600 released Jan-2023
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage

---

### Performance Results

**CPU2017 License:** 9019
**Test Sponsor:** Cisco Systems
**Tested by:** Cisco Systems
**Test Date:** Mar-2023
**Hardware Availability:** Mar-2023
**Software Availability:** Dec-2022

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>128</td>
<td>862</td>
<td>921</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>64</td>
<td>921</td>
<td>921</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>128</td>
<td>333</td>
<td>330</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>64</td>
<td>430</td>
<td>430</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>128</td>
<td>689</td>
<td>715</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>128</td>
<td>349</td>
<td>349</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>64</td>
<td>541</td>
<td>538</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>128</td>
<td>654</td>
<td>654</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>64</td>
<td>699</td>
<td>699</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>128</td>
<td>1900</td>
<td></td>
</tr>
<tr>
<td>544.nab_r</td>
<td>128</td>
<td>1290</td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>128</td>
<td>534</td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>64</td>
<td>309</td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>64</td>
<td>324</td>
<td></td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base = 703**
**SPECrate®2017_fp_peak = 722**
## Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>128</td>
<td>385</td>
<td>3330</td>
<td>386</td>
<td>3320</td>
<td>386</td>
<td>3330</td>
<td>128</td>
<td>385</td>
<td>3330</td>
<td>386</td>
<td>3320</td>
<td>386</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>128</td>
<td>188</td>
<td>861</td>
<td>188</td>
<td>864</td>
<td>188</td>
<td>862</td>
<td>64</td>
<td>88.2</td>
<td>919</td>
<td>87.8</td>
<td>922</td>
<td>88.0</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>128</td>
<td>275</td>
<td>442</td>
<td>275</td>
<td>442</td>
<td>275</td>
<td>442</td>
<td>128</td>
<td>275</td>
<td>442</td>
<td>275</td>
<td>442</td>
<td>275</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>128</td>
<td>1004</td>
<td>333</td>
<td>1005</td>
<td>333</td>
<td>1003</td>
<td>334</td>
<td>64</td>
<td>439</td>
<td>430</td>
<td>390</td>
<td>430</td>
<td>390</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>128</td>
<td>432</td>
<td>691</td>
<td>435</td>
<td>687</td>
<td>434</td>
<td>689</td>
<td>128</td>
<td>419</td>
<td>713</td>
<td>418</td>
<td>716</td>
<td>418</td>
</tr>
<tr>
<td>519.ibm_r</td>
<td>128</td>
<td>386</td>
<td>349</td>
<td>386</td>
<td>349</td>
<td>387</td>
<td>349</td>
<td>128</td>
<td>386</td>
<td>349</td>
<td>386</td>
<td>349</td>
<td>387</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>128</td>
<td>530</td>
<td>541</td>
<td>529</td>
<td>542</td>
<td>532</td>
<td>539</td>
<td>64</td>
<td>258</td>
<td>557</td>
<td>257</td>
<td>558</td>
<td>255</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>128</td>
<td>298</td>
<td>655</td>
<td>298</td>
<td>654</td>
<td>298</td>
<td>654</td>
<td>128</td>
<td>298</td>
<td>655</td>
<td>298</td>
<td>654</td>
<td>298</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>128</td>
<td>319</td>
<td>702</td>
<td>320</td>
<td>699</td>
<td>321</td>
<td>698</td>
<td>64</td>
<td>175</td>
<td>641</td>
<td>175</td>
<td>641</td>
<td>179</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>128</td>
<td>168</td>
<td>1900</td>
<td>167</td>
<td>1900</td>
<td>167</td>
<td>1900</td>
<td>128</td>
<td>168</td>
<td>1900</td>
<td>167</td>
<td>1900</td>
<td>167</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>128</td>
<td>167</td>
<td>1290</td>
<td>167</td>
<td>1290</td>
<td>166</td>
<td>1300</td>
<td>128</td>
<td>167</td>
<td>1290</td>
<td>167</td>
<td>1290</td>
<td>166</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>128</td>
<td>934</td>
<td>534</td>
<td>933</td>
<td>534</td>
<td>934</td>
<td>534</td>
<td>128</td>
<td>934</td>
<td>534</td>
<td>934</td>
<td>534</td>
<td>934</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>128</td>
<td>661</td>
<td>307</td>
<td>659</td>
<td>309</td>
<td>659</td>
<td>309</td>
<td>64</td>
<td>314</td>
<td>324</td>
<td>315</td>
<td>323</td>
<td>314</td>
</tr>
</tbody>
</table>

### Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

### General Notes
Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM memory using Red Hat Enterprise Linux 8.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
General Notes (Continued)

sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numaclt i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Sub NUMA Clustering set to Enable SNC4
LLC Dead Line set to Disabled
ADDDC Sparing set to Disabled
Processor C6 Report set to Enabled
UPI Link Enablement 3
UPI Link Power Management Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6732 of 2022-11-07 fe91c8b7ed5c36ae2c92cc097bec197
running on srv04 Mon Mar  6 06:47:55 2023

SUT (System Under Test) info as seen by some common utilities.

Table of contents

1. uname -a
2. w
3. Username
4. ulimit -a
5. sysinfo process ancestry
6. /proc/cpurnfo
7. lscpu
8. numaclt --hardware
9. /proc/meminfo
10. who -r
11. Systemd service manager version: systemd 249 (249.11+suse.124.g2bc0b2c447)
12. Services, from systemctl list-unit-files
13. Linux kernel boot-time arguments, from /proc/cmdline

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

### Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

| SPECrate®2017_fp_base = 703 | SPECrate®2017_fp_peak = 722 |

| CPU2017 License: | 9019 |
| Test Sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |

| Test Date: | Mar-2023 |
| Hardware Availability: | Mar-2023 |
| Software Availability: | Dec-2022 |

### Platform Notes (Continued)

14. cpupower frequency-info
15. sysctl
16. /sys/kernel/mm/transparent_hugepage
17. /sys/kernel/mm/transparent_hugepage/khugepaged
18. OS release
19. Disk information
20. /sys/devices/virtual/dmi/id
21. dmidecode
22. BIOS

---

1. uname -a
   
   Linux srv04 5.14.21-150400.22-default #1 SMP PREEMPT_DYNAMIC Wed May 11 06:57:18 UTC 2022 (49db222) x86_64
   x86_64 x86_64 GNU/Linux

---

2. w
   
   06:47:55 up 4 min,  1 user,  load average: 0.28, 1.12, 0.62
   USER     TTY      FROM             LOGIN@   IDLE   JCPU   PCPU WHAT
   root     tty1     -                06:47   11.00s  1.05s  0.16s -bash

---

3. Username
   
   From environment variable $USER: root

---

4. ulimit -a
   
   core file size          (blocks, -c) unlimited
   data seg size           (kbytes, -d) unlimited
   scheduling priority             (-e) 0
   file size               (blocks, -f) unlimited
   pending signals                 (-i) 4126812
   max locked memory       (kbytes, -l) 64
   max memory size         (kbytes, -m) unlimited
   open files                      (-n) 1024
   pipe size            (512 bytes, -p) 8
   POSIX message queues     (bytes, -q) 819200
   real-time priority              (-r) 0
   stack size              (kbytes, -s) unlimited
   cpu time               (seconds, -t) unlimited
   max user processes       (-u) 4126812
   virtual memory         (kbytes, -v) unlimited
   file locks                      (-x) unlimited

---

5. sysinfo process ancestry

(Continued on next page)
Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

SPECrate®2017_fp_base = 703
SPECrate®2017_fp_peak = 722

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Mar-2023
Hardware Availability: Mar-2023
Software Availability: Dec-2022

Platform Notes (Continued)

/usr/lib/systemd/systemd --switched-root --system --deserializer 30
login -- root
-bash
-bash
runcpu --nobuild --action validate --define default-platform-flags --define numcopies=128 --configfile ic2023.0-lin-sapphirerapids-rate-20221201.cfg --reportable --iterations 3 --define smt-on --define cores=64 --define physicalfirst --define invoke_with_interleave --define drop_caches --tune all -o all fprate
runcpu --nobuild --action validate --define default-platform-flags --define numcopies=128 --configfile ic2023.0-lin-sapphirerapids-rate-20221201.cfg --reportable --iterations 3 --define smt-on --define cores=64 --define physicalfirst --define invoke_with_interleave --define drop_caches --tune all --output_format all --nopower --runmode rate --tune base:peak --size reframe fprate --nopreenv --note-preenv --logfile $SPEC/tmp/CPU2017.161/templogs/preenv.fprate.161.0.log --lognum 161.0 --from_runcpu 2
specperl $SPEC/bin/sysinfo
$SPEC = /home/cpu2017

------------------------------------------------------------
6. /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6448Y
vendor_id : GenuineIntel
cpu family : 6
model : 143
stepping : 8
microcode : 0x2b000161
bugs : spectre_v1 spectre_v2 spec_store_bypass swapgs
cpu cores : 32
siblings : 64
2 physical ids (chips)
128 processors (hardware threads)
physical id 0: core ids 0-31
physical id 1: core ids 0-31
physical id 0: apicids 0-63
physical id 1: apicids 128-191
Caution: /proc/cpuinfo data regarding chips, cores, and threads is not necessarily reliable, especially for virtualized systems. Use the above data carefully.

------------------------------------------------------------
7. lscpu

From lscpu from util-linux 2.37.2:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Address sizes: 46 bits physical, 57 bits virtual
Byte Order: Little Endian
CPU(s): 128
On-line CPU(s) list: 0-127

(Continued on next page)
Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 703</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = 722</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

<table>
<thead>
<tr>
<th>Vendor ID:</th>
<th>GenuineIntel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model name:</td>
<td>Intel(R) Xeon(R) Gold 6448Y</td>
</tr>
<tr>
<td>CPU family:</td>
<td>6</td>
</tr>
<tr>
<td>Model:</td>
<td>143</td>
</tr>
<tr>
<td>Thread(s) per core:</td>
<td>2</td>
</tr>
<tr>
<td>Core(s) per socket:</td>
<td>32</td>
</tr>
<tr>
<td>Socket(s):</td>
<td>2</td>
</tr>
<tr>
<td>Stepping:</td>
<td>8</td>
</tr>
<tr>
<td>CPU max MHz:</td>
<td>4100.0000</td>
</tr>
<tr>
<td>CPU min MHz:</td>
<td>800.0000</td>
</tr>
<tr>
<td>BogoMIPS:</td>
<td>4200.00</td>
</tr>
</tbody>
</table>

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 ciferush ds cpl vm xsaes vm xset tm2 ssse3 sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant tsx arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmu smx est tm2 ssse3 sse2 sse txr pdcm pcd dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dmnowprefetch cpuid_fault epb cat_l3 cat_l2 cdp_l3 invpcid_single intel_pni cca cpdp_l2 ssbd mbx ibrs ibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bni mle avx2 smep bmi2 erms invpcid rtm cmq rdt_a avx512f avx512dq rdseed adx smap avx512ifma cfi十条hp intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsaves xsave esm cmqm llc cmq_occupa llc cmq_mbm_total cmq_mbm_local split lock detect avx vmmi avx512佈16 wbnoinvd dtherm ida arat pin pts hwp hwp act_window hwp_erep hwp_pkg req avx512vmbi umip pku ospke waitpkg avx512_vmbi gfn vaes vpcmuleq avx vmmi avx512 vbitaalg tme avx512 vpuncntdq 1a57 rdpid bus_lock_detect c1d ncpu movdir movdir64b enqcmd fnm _clear serialize tsxldtrc pconf carch _ibr avx512_fp16 amx_tle flush_l1d arch_capabilities

Virtualization: VT-x
L1d cache: 3 MiB (64 instances)
L1i cache: 2 MiB (64 instances)
L2 cache: 128 MiB (64 instances)
L3 cache: 120 MiB (2 instances)
NUMA node(s): 4
NUMA node0 CPU(s): 0-15, 64-79
NUMA node1 CPU(s): 16-31, 80-95
NUMA node2 CPU(s): 32-47, 96-111
NUMA node3 CPU(s): 48-63, 112-127
Vulnerability Itlb multihit: Not affected
Vulnerability Llft: Not affected
Vulnerability Mds: Not affected
Vulnerability Meltdown: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitization
Vulnerability Spectre v2: Mitigation; Enhanced IBRS, IBP conditional, RSB filling
Vulnerability Srbds: Not affected

(Continued on next page)
Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)  SPECrate®2017_fp_base = 703
SPECrate®2017_fp_peak = 722

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  

Test Date: Mar-2023  
Hardware Availability: Mar-2023  
Software Availability: Dec-2022

Platform Notes (Continued)

Vulnerability Tsx async abort:  Not affected

From lscpu --cache:

<table>
<thead>
<tr>
<th>NAME</th>
<th>ONE-SIZE</th>
<th>ALL-SIZE</th>
<th>WAYS</th>
<th>TYPE</th>
<th>LEVEL</th>
<th>SETS</th>
<th>PHY-LINE</th>
<th>COHERENCY-SIZE</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1d</td>
<td>48K</td>
<td>3M</td>
<td>12</td>
<td>Data</td>
<td>1</td>
<td>64</td>
<td>1</td>
<td>64</td>
</tr>
<tr>
<td>L1i</td>
<td>32K</td>
<td>2M</td>
<td>8</td>
<td>Instruction</td>
<td>1</td>
<td>64</td>
<td>1</td>
<td>64</td>
</tr>
<tr>
<td>L2</td>
<td>2M</td>
<td>128M</td>
<td>16</td>
<td>Unified</td>
<td>2</td>
<td>2048</td>
<td>1</td>
<td>64</td>
</tr>
<tr>
<td>L3</td>
<td>60M</td>
<td>120M</td>
<td>15</td>
<td>Unified</td>
<td>3</td>
<td>65536</td>
<td>1</td>
<td>64</td>
</tr>
</tbody>
</table>

8. numactl --hardware
NOTE: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0-15,64-79
node 0 size: 257688 MB
node 0 free: 255894 MB
node 1 cpus: 16-31,80-95
node 1 size: 258005 MB
node 1 free: 256895 MB
node 2 cpus: 32-47,96-111
node 2 size: 258039 MB
node 2 free: 256904 MB
node 3 cpus: 48-63,112-127
node 3 size: 257992 MB
node 3 free: 256909 MB
node distances:
node   0   1   2   3
0: 10 12 21 21
1: 12 10 21 21
2: 21 21 10 12
3: 21 21 12 10

9. /proc/meminfo
MemTotal: 1056488488 kB

10. who -r
run-level 3 Mar 6 06:44

11. Systemd service manager version: systemd 249 (249.11+suse.124.g2bc0b2c447)
Default Target Status
multi-user running

12. Services, from systemctl list-unit-files

(Continued on next page)
Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 703
SPECrate®2017_fp_peak = 722

Platform Notes (Continued)

STATE UNIT FILES
enabled YaST2-Firstboot YaST2-Second-Stage apparmor auditd cron getty@ haveged irqbalance
issue-generator kbdsettings lvm2-monitor nscd postfix purge-kernels rollback rsyslog
smartd sshd wicked wickedd-auto4 wickedd-dhcp4 wickedd-dhcp6 wickedd-nanny
enabled-runtime systemd-remount-fs
disabled autofs autoyast-initscripts blk-availability boot-sysctl ca-certificates chrony-wait
chronyd console-getty cups cups-browsed debug-shell ebtables exchange-bmc-os-info
firewalld gpm grub2-once haveged-switch-root ipmi ipmievd issue-add-ssh-keys kexec-load
lunmask man-db-create multipathd nscd nfs nfs-blkmap rdisc rpcbind rpmconfigcheck rsysncd
serial-getty@ smartd_generate_opts snmpd snmptrapd svnserve systemd-boot-check-no-failures
systemd-network-generator systemd-sysext systemd-time-wait-sync systemd-timesyncd udisks2
indirect wickedd

13. Linux kernel boot-time arguments, from /proc/cmdline

BOOT_IMAGE=/boot/vmlinuz-5.14.21-150400.22-default
root=UUID=e05292c4-0a31-46de-94f3-3ad8c6a360dd
splash=silent
mitigations=auto
quiet
security=

14. cpupower frequency-info

analyzing CPU 0:

current policy: frequency should be within 800 MHz and 4.10 GHz.
The governor "performance" may decide which speed to use
within this range.

boost state support:
Supported: yes
Active: yes

15. sysctl

kernel.numa_balancing 0
kernel.randomize_va_space 2
vm.compaction_proactiveness 20
vm.dirty_background_bytes 0
vm.dirty_background_ratio 10
vm.dirty_bytes 0
vm.dirty_expire_centisecs 3000
vm.dirty_ratio 20
vm.dirty_writeback_centisecs 500
vm.dirtytime_expire_seconds 43200
vm.extfrag_threshold 500
vm.min_unmapped_ratio 1
vm.nr_hugepages 0

(Continued on next page)
Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)  

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Mar-2023  
Hardware Availability: Mar-2023  
Software Availability: Dec-2022  

Platform Notes (Continued)

vm.nr_hugepages_mempolicy 0  
vm.nr_overcommit_hugepages 0  
vm.swappiness 1  
vm.watermark_boost_factor 15000  
vm.watermark_scale_factor 10  
vm.zone_reclaim_mode 0

----------------------------------------
16. /sys/kernel/mm/transparent_hugepage
   defrag [always] defer defer+madvise madvise never
   enabled [always] madvise never
   hpage_pmd_size 2097152
   shmem_enabled always within_size advise [never] deny force

----------------------------------------
17. /sys/kernel/mm/transparent_hugepage/khugepaged
   alloc_sleep_millisecs 60000
   defrag 1
   max_ptes_none 511
   max_ptes_shared 256
   max_ptes_swap 64
   pages_to_scan 4096
   scan_sleep_millisecs 10000

----------------------------------------
18. OS release
   From /etc/*-release /etc/*-version
   os-release SUSE Linux Enterprise Server 15 SP4

----------------------------------------
19. Disk information
   SPEC is set to: /home/cpu2017
   Filesystem     Type  Size  Used Avail Use% Mounted on
   /dev/sdb3      xfs   218G  11G  208G   5% /

----------------------------------------
20. /sys/devices/virtual/dmi/id
   Vendor: Cisco Systems Inc
   Product: UCSC-C240-M7SX
   Serial: WZP263592NZ

----------------------------------------
21. dmidecode
   Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)
# SPEC CPU®2017 Floating Point Rate Result

## Cisco Systems

Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>703</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>722</td>
</tr>
</tbody>
</table>

- **CPU2017 License:** 9019
- **Test Sponsor:** Cisco Systems
- **Tested by:** Cisco Systems
- **Test Date:** Mar-2023
- **Hardware Availability:** Mar-2023
- **Software Availability:** Dec-2022

### Platform Notes (Continued)

Memory:

16x 0xAD00 HMCG94MEBRA109N 64 GB 2 rank 4800

---

### 22. BIOS

(This section combines info from /sys/devices and dmidecode.)

<table>
<thead>
<tr>
<th>BIOS Vendor</th>
<th>Cisco Systems, Inc.</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIOS Version</td>
<td>C240M7.4.2.600.594.0120230612</td>
</tr>
<tr>
<td>BIOS Date</td>
<td>01/20/2023</td>
</tr>
<tr>
<td>BIOS Revision</td>
<td>5.29</td>
</tr>
</tbody>
</table>

### Compiler Version Notes

---

### C

| 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak) |

---

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2023.0.0 Build 20221201

Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

---

### C++

| 508.namd_r(base, peak) 510.parest_r(base, peak) |

---

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2023.0.0 Build 20221201

Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

---

### C++, C

| 511.povray_r(base, peak) 526.blender_r(base, peak) |

---

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2023.0.0 Build 20221201

Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

---

### C++, C, Fortran

| 507.cactuBSSN_r(base, peak) |

---

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

SPECrater®2017_fp_base = 703
SPECrater®2017_fp_peak = 722

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Mar-2023
Hardware Availability: Mar-2023
Software Availability: Dec-2022

Compiler Version Notes (Continued)

Version 2023.0.0 Build 20221201
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2023.0.0 Build 20221201
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version
2023.0.0 Build 20221201
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

==============================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
| 554.roms_r(base, peak)
==============================================================================

Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version
2023.0.0 Build 20221201
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
==============================================================================

Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version
2023.0.0 Build 20221201
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2023.0.0 Build 20221201
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.

==============================================================================

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifx

Benchmarks using both Fortran and C:
ifx icx

Benchmarks using both C and C++:
icpx icx

(Continued on next page)
Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

SPECrate®2017_fp_base = 703
SPECrate®2017_fp_peak = 722

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Mar-2023
Hardware Availability: Mar-2023
Software Availability: Dec-2022

Base Compiler Invocation (Continued)

Benchmarks using Fortran, C, and C++:
icpx icx ifx

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xsapphirerapids -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-Wno-implicit-int -mprefer-vector-width=512 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
-w -std=c++14 -m64 -Wl,-z,muldefs -xsapphirerapids -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mprefer-vector-width=512 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xsapphirerapids -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

(Continued on next page)
Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2023 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

SPECrate®2017_fp_base = 703
SPECrate®2017_fp_peak = 722

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Mar-2023
Hardware Availability: Mar-2023
Software Availability: Dec-2022

Base Optimization Flags (Continued)
Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xsapphirerapids -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-Wno-implicit-int -mprefer-vector-width=512 -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -std=c++14 -m64 -std=c11 -Wl,-z,muldefs -xsapphirerapids -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -Wno-implicit-int -mprefer-vector-width=512
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c++14 -std=c11 -Wl,-z,muldefs -xsapphirerapids -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -Wno-implicit-int -mprefer-vector-width=512
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Peak Compiler Invocation
C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifx

Benchmarks using both Fortran and C:
ifx icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifx
Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2023 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

SPECrate®2017_fp_base = 703
SPECrate®2017_fp_peak = 722

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Mar-2023
Tested by: Cisco Systems
Hardware Availability: Mar-2023
Software Availability: Dec-2022

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags
C benchmarks:
519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: basepeak = yes

C++ benchmarks:
508.namd_r: basepeak = yes
510.parest_r -w -std=c++14 -m64 -Wl,-z,muldefs -xsapphirerapids
-Ofast -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mprefer-vector-width=512
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
503.bwaves_r: basepeak = yes
549.fotonik3d_r: basepeak = yes
554.roms_r -w -m64 -Wl,-z,muldefs -xsapphirerapids -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xsapphirerapids -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-Wno-implicit-int -mprefer-vector-width=512 -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
511.povray_r -w -std=c++14 -m64 -std=c11 -Wl,-z,muldefs
-fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2(pass 1)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M7 (Intel Xeon Gold 6448Y, 2.10GHz)

SPECrate®2017_fp_base = 703
SPECrate®2017_fp_peak = 722

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Mar-2023
Hardware Availability: Mar-2023
Software Availability: Dec-2022

Peak Optimization Flags (Continued)

511.povray_r (continued):
-ffast-math -flto -Ofast -xCORE-AVX512 -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -Wno-implicit-int
-mprefer-vector-width=512 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

526.blender_r.basepeak = yes

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c++14 -std=c11 -Wl,-z,muldefs -xsapphirerapids -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -Wno-implicit-int -mprefer-vector-width=512
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2023-official-linux64.xml

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic2023-official-linux64.html

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.9 on 2023-03-06 09:47:55-0500.
Report generated on 2023-03-29 00:36:05 by CPU2017 PDF formatter v6442.
Originally published on 2023-03-28.