Cisco Systems
Cisco UCS X210 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrinate®2017_int_base = 428
SPECrinate®2017_int_peak = 441

Hardware
CPU Name: Intel Xeon Silver 4516Y+
Max MHz: 3700
Nominal: 2200
Enabled: 48 cores, 2 chips, 2 threads/core
Orderable: 1.2 chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 2 MB I+D on chip per core
L3: 45 MB I+D on chip per chip
Other: None
Memory: 1 TB (16 x 64 GB 2Rx4 PC5-5600B-R, running at 4400)
Storage: 1 x 960 GB SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 SP4
Kernel 5.14.21-150400.22-default
Compiler: C/C++: Version 2023.2.3 of Intel oneAPI DPC++/C++
Compiler for Linux:
Fortran: Version 2023.2.3 of Intel Fortran
Compiler for Linux:
Parallel: No
Firmware: Version 4.3.3a released Jan-2024
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
## SPEC CPU®2017 Integer Rate Result

### Cisco Systems

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<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
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<td>Cisco Systems</td>
</tr>
</tbody>
</table>

---

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>96</td>
<td>456</td>
<td>335</td>
<td>456</td>
<td>335</td>
<td>456</td>
<td>96</td>
<td>419</td>
<td>365</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>96</td>
<td>360</td>
<td>377</td>
<td>362</td>
<td>375</td>
<td>365</td>
<td>96</td>
<td>305</td>
<td>445</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>96</td>
<td>220</td>
<td>706</td>
<td>220</td>
<td>706</td>
<td>220</td>
<td>96</td>
<td>220</td>
<td>704</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>96</td>
<td>453</td>
<td>278</td>
<td>453</td>
<td>278</td>
<td>452</td>
<td>96</td>
<td>453</td>
<td>278</td>
</tr>
<tr>
<td>523.xalanbmk_r</td>
<td>96</td>
<td>178</td>
<td>568</td>
<td>178</td>
<td>568</td>
<td>178</td>
<td>96</td>
<td>178</td>
<td>568</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>96</td>
<td>191</td>
<td>879</td>
<td>191</td>
<td>879</td>
<td>191</td>
<td>96</td>
<td>182</td>
<td>926</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>96</td>
<td>353</td>
<td>312</td>
<td>353</td>
<td>312</td>
<td>353</td>
<td>96</td>
<td>353</td>
<td>312</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>96</td>
<td>545</td>
<td>291</td>
<td>546</td>
<td>291</td>
<td>545</td>
<td>96</td>
<td>545</td>
<td>291</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>96</td>
<td>282</td>
<td>892</td>
<td>282</td>
<td>892</td>
<td>285</td>
<td>96</td>
<td>282</td>
<td>892</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>96</td>
<td>496</td>
<td>209</td>
<td>502</td>
<td>207</td>
<td>504</td>
<td>96</td>
<td>496</td>
<td>209</td>
</tr>
</tbody>
</table>

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"
```

### General Notes

- Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM memory using Red Hat Enterprise Linux 8.4
- Transparent Huge Pages enabled by default
- Prior to runcpu invocation:
  - Filesystem page cache synced and cleared with:
    - `sync; echo 3 > /proc/sys/vm/drop_caches`
  - runcpu command invoked through numactl i.e.:
    - `numactl --interleave=all runcpu <etc>`
- NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
- Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
- Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
General Notes (Continued)

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Sub NUMA Clustering set to Enable SNC2 (2-clusters)
Adjacent cache line prefetcher set to Enabled
DCU streamer prefetch set to Disabled
Enhanced CPU performance set to Auto
LLC Dead Line set to Disabled
Processor C6 Report set to Enabled
ADDDC Sparing set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6732 of 2022-11-07 fe91c89b7ed5c36ae2c92cc097bec197
running on emr-x210-spec Sat Feb 24 18:15:52 2024

SUT (System Under Test) info as seen by some common utilities.

------------------------------------------------------------
Table of contents
------------------------------------------------------------
1. uname -a
2. w
3. Username
4. ulimit -a
5. sysinfo process ancestry
6. /proc/cpuinfo
7. lscpu
8. numactl --hardware
9. /proc/meminfo
10. who -r
11. Systemd service manager version: systemd 249 (249.11+suse.124.g2bc0b2c447)
12. Services, from systemctl list-unit-files
13. Linux kernel boot-time arguments, from /proc/cmdline
14. cpupower frequency-info
15. sysctl
16. /sys/kernel/mm/transparent_hugepage
17. /sys/kernel/mm/transparent_hugepage/khugepaged
18. OS release
19. Disk information
20. /sys/devices/virtual/dmi/id
21. dmidecode
22. BIOS
------------------------------------------------------------

1. uname -a
Linux emr-x210-spec 5.14.21-150400.22-default #1 SMP PREEMPT_DYNAMIC Wed May 11 06:57:18 UTC 2022 (49db222)
x86_64 x86_64 x86_64 GNU/Linux

2. w
18:15:52 up 6 min, 1 user, load average: 0.42, 1.02, 0.65
USER TTY FROM LOGIN@ IDLE JCPU PCPU WHAT
root tty1 - 18:10 8.00s 1.75s 0.20s -bash

(Continued on next page)
Platform Notes (Continued)

3. Username
   From environment variable $USER: root

4. ulimit -a
   core file size (blocks, -c) unlimited
   data seg size (kbytes, -d) unlimited
   scheduling priority (-e) 0
   file size (blocks, -f) unlimited
   pending signals (-i) 4126862
   max locked memory (kbytes, -l) 64
   max memory size (kbytes, -m) unlimited
   open files (-n) 1024
   pipe size (512 bytes, -p) 8
   POSIX message queues (bytes, -q) 819200
   real-time priority (-r) 0
   stack size (kbytes, -s) unlimited
   cpu time (seconds, -t) unlimited
   max user processes (-u) 4126862
   virtual memory (kbytes, -v) unlimited
   file locks (-x) unlimited

5. sysinfo process ancestry
   /usr/lib/systemd/systemd --switched-root --system --deserialize 30
   login -- root
   -bash
   sh runrate.ic2023.sh
   runcpu --nobuild --action validate --define default-platform-flags --define numcopies=96 -c
   ic2023.2.3-lin-sapphirerapids-rate-20231121.cfg --reportable --iterations 3 --define smt-on --define
   cores=48 --define physicalfirst --define invoke_with_interleave --define drop_caches --tune all --all
   intrate
   runcpu --nobuild --action validate --define default-platform-flags --define numcopies=96 --configfile
   ic2023.2.3-lin-sapphirerapids-rate-20231121.cfg --reportable --iterations 3 --define smt-on --define
   cores=48 --define physicalfirst --define invoke_with_interleave --define drop_caches --tune all
   --output_format all --nopower --runmode rate --tune base:peak --size refrate intrate --nopreenv
   --note-preenv --logfile $SPEC/tmp/CPU2017.007/templogs/preenv.intrate.007.0.log --lognum 007.0
   --from_runcpu 2
   specperl $SPEC/bin/sysinfo
   $SPEC = /home/cpu2017

6. /proc/cpuinfo
   model name : INTEL(R) XEON(R) SILVER 4516Y+
   vendor_id : GenuineIntel
   cpu family : 6
   model : 207
   stepping : 2
   microcode : 0x21000200
   bugs : spectre_v1 spectre_v2 spec_store_bypass swapgs
   cpu cores : 24
   siblings : 48
   2 physical ids (chips)
   96 processors (hardware threads)
   physical id 0: core ids 0-23
   physical id 1: core ids 0-23
   physical id 0: apicids 0-47
   physical id 1: apicids 128-175

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CPU op-mode(s): 32-bit, 64-bit
Address sizes: 46 bits physical, 57 bits virtual
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Vendor ID: GenuineIntel
Model name: INTEL(R) XEON(R) SILVER 4516Y+
CPU family: 6
Model: 207
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
Stepping: 2
CPU max MHz: 3700.0000
CPU min MHz: 800.0000
BogoMIPS: 4400.00
Flags: fpu vme de pse mce cmov pat pse36
clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant-tsc arch_perfmon pebs bts rep_good nopl xtopology
nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor
srse cpuid_fault epb cat_l1d cat_l1i cd gsa

Platform Notes (Continued)

Caution: /proc/cpuinfo data regarding chips, cores, and threads is not necessarily reliable, especially for virtualized systems. Use the above data carefully.

7. lscpu

From lscpu from util-linux 2.37.2:

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Address sizes: 46 bits physical, 57 bits virtual
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Vendor ID: GenuineIntel
Model name: INTEL(R) XEON(R) SILVER 4516Y+
CPU family: 6
Model: 207
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
Stepping: 2
CPU max MHz: 3700.0000
CPU min MHz: 800.0000
BogoMIPS: 4400.00
Flags: fpu vme de pse mce cmov pat pse36
clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant-tsc arch_perfmon pebs bts rep_good nopl xtopology
nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor
srse cpuid_fault epb cat_l1d cat_l1i cd gsa

Virtualization:
VT-x
L1d cache: 2.3 MiB (48 instances)
L1i cache: 1.5 MiB (48 instances)
L2 cache: 96 MiB (48 instances)
L3 cache: 90 MiB (2 instances)
NUMA node(s): 4
NUMA node0 CPU(s): 0-11,48-59
NUMA node1 CPU(s): 12-23,60-71
NUMA node2 CPU(s): 24-35,72-83
NUMA node3 CPU(s): 36-47,84-95

Vulnerability Itlb multihit: Not affected
Vulnerability L1tf: Not affected
Vulnerability Mds: Not affected
Vulnerability Meltdown: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swaps barriers and __user pointer sanitization
Vulnerability Spectre v2: Mitigation; Enhanced IBRS, IBPB conditional, RSB filling
Vulnerability Srbds: Not affected

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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SPECrate®2017_int_base = 428
SPECrate®2017_int_peak = 441

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

Vulnerability Tx async abort: Not affected

From lscpu --cache:

<table>
<thead>
<tr>
<th>NAME</th>
<th>ONE-SIZE</th>
<th>ALL-SIZE</th>
<th>WAYS</th>
<th>TYPE</th>
<th>LEVEL</th>
<th>SETS</th>
<th>PHY-LINE</th>
<th>COHERENCY-SIZE</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1d</td>
<td>48K</td>
<td>2.3M</td>
<td>12</td>
<td>Data</td>
<td>1</td>
<td>64</td>
<td>1</td>
<td>64</td>
</tr>
<tr>
<td>L1i</td>
<td>32K</td>
<td>1.5M</td>
<td>8</td>
<td>Instruction</td>
<td>1</td>
<td>64</td>
<td>1</td>
<td>64</td>
</tr>
<tr>
<td>L2</td>
<td>2M</td>
<td>90M</td>
<td>16</td>
<td>Unified</td>
<td>2</td>
<td>2048</td>
<td>1</td>
<td>64</td>
</tr>
<tr>
<td>L3</td>
<td>45M</td>
<td>90M</td>
<td>15</td>
<td>Unified</td>
<td>3</td>
<td>49152</td>
<td>1</td>
<td>64</td>
</tr>
</tbody>
</table>

8. numactl --hardware
NOTE: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0-11,48-59
node 0 size: 257677 MB
node 0 free: 256752 MB
node 1 cpus: 12-23,60-71
node 1 size: 258041 MB
node 1 free: 257656 MB
node 2 cpus: 24-35,72-83
node 2 size: 258007 MB
node 2 free: 257638 MB
node 3 cpus: 36-47,84-95
node 3 size: 258012 MB
node 3 free: 257625 MB
node distances:
node 0   1   2   3
0: 10  12  21  21
1: 12  10  21  21
2: 21  21  10  12
3: 21  21  12  10

9. /proc/meminfo
MemTotal: 1056501240 kB

10. who -r
run-level 3 Feb 24 18:09

11. Systemd service manager version: systemd 249 (249.11+suse.124.g2bc0b2c447)
Default Target running

12. Services, from systemctl list-unit-files
STATE FILES
enabled Yast2-Firstboot Yast2-Second-Stage auditd cron getty@ havedeg irqbalance issue-generator kbdsettings klog lvm2-monitor nscd nvme-fc-boot-connections postfix purge-kernels rollback rsyslog smartd sshd wicked wicked-auto4 wicked-dhcp4 wicked-dhcp6 wickedd-nanny
enabled-runtime systemctl-remount-fs
indirect systemd-time-wait-sync systemd-sysextd udisks2
wickedd

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Platform Notes (Continued)

13. Linux kernel boot-time arguments, from /proc/cmdline
   BOOT_IMAGE=/boot/vmlinuz-5.14.21-150400.22-default
   root=UUID=72058f1f-355b-4421-909c-1facaea01bdc
   splash=silent
   mitigations=auto
   quiet
   security=

14. cpupower frequency-info
   analyzing CPU 0:
   current policy: frequency should be within 800 MHz and 3.70 GHz.
   The governor "performance" may decide which speed to use
   within this range.
   boost state support:
   Supported: yes
   Active: yes

15. sysctl
   kernel.numa_balancing 1
   kernel.randomize_va_space 2
   vm.compaction_proactiveness 20
   vm.dirty_background_bytes 0
   vm.dirty_background_ratio 10
   vm.dirty_bytes 0
   vm.dirty_expire_centisecs 3000
   vm.dirty_ratio 20
   vm.dirty_writeback_centisecs 500
   vm.dirtytime_expire_seconds 43200
   vm.extfrag_threshold 500
   vm.min_unmapped_ratio 1
   vm.nr_hugepages 0
   vm.nr_hugepages_mempolicy 0
   vm.nr_overcommit_hugepages 0
   vm.swappiness 1
   vm.watermark_boost_factor 15000
   vm.watermark_scale_factor 10
   vm.zone_reclaim_mode 0

16. /sys/kernel/mm/transparent_hugepage
   defrag always defer defer+madvis[e [madvis[e never
   enabled [always] madvis[e never
   hpage_pmd_size 2097152
   shmem_enabled always within_size advise [never] deny force

17. /sys/kernel/mm/transparent_hugepage/khugepaged
   alloc_sleep_millisecs 60000
   defrag 1
   max_ptes_none 511
   max_ptes_shared 256
   max_ptes_swap 64
   pages_to_scan 4096
   scan_sleep_millisecs 10000

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Test Date: Feb-2024
Hardware Availability: Feb-2024
Software Availability: Dec-2023

Platform Notes (Continued)

18. OS release
   From /etc/*-release /etc/*-version
   os-release SUSE Linux Enterprise Server 15 SP4

19. Disk information
   SPEC is set to: /home/cpu2017
   Filesystem  Type  Size  Used Avail Use% Mounted on
   /dev/sdb2      xfs   893G   16G  878G   2% /

20. /sys/devices/virtual/dmi/id
   Vendor: Cisco Systems Inc
   Product: UCSX-210C-M7
   Serial: FCH270177DF

21. dmidecode
   Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section.
   The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately
   determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the
   "DMTF SMBIOS" standard.
   Memory:
   16x 0xCE00 M321R8GA0PB0-CWMCH 64 GB 2 rank 5600, configured at 4400

22. BIOS
   (This section combines info from /sys/devices and dmidecode.)
   BIOS Vendor: Cisco Systems, Inc.
   BIOS Version: X210M7.4.3.38 Version 0.0118241337
   BIOS Date: 01/18/2024
   BIOS Revision: 5.32

Compiler Version Notes

C | 502.gcc_r(peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2023.2.3 Build x
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.

C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak)
   557.xz_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2023.2.3 Build x
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.

C | 502.gcc_r(peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2023.2.3 Build x
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Compiler Version Notes (Continued)

C
| 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak)
| 557.xz_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2023.2.3 Build x
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.

C++
| 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak) 531.deepsjeng_r(base, peak)
| 541.leela_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2023.2.3 Build x
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.

Fortran
| 548.exchange2_r(base, peak)

Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 2023.2.3 Build x
Copyright (C) 1985-2023 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx
C++ benchmarks:
icpx
Fortran benchmarks:
ifx

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
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---

**Base Optimization Flags**

C benchmarks:
- `-w -std=gnu11 -m64 -Wl,-z,muldefs -xsapphirerapids -O3 -ffast-math`
- `-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-L/home/specdev/new_compilers/ic2023.2.3/compiler/lib/intel64_lin`
- `-lqkmalloc`

C++ benchmarks:
- `-w -std=c++14 -m64 -Wl,-z,muldefs -xsapphirerapids -O3 -ffast-math`
- `-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-L/home/specdev/new_compilers/ic2023.2.3/compiler/lib/intel64_lin`
- `-lqkmalloc`

Fortran benchmarks:
- `-w -m64 -Wl,-z,muldefs -xsapphirerapids -O3 -ffast-math -flto`
- `-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4`
- `-nostandard-realloc-lhs -align array32byte -auto`
- `-L/home/specdev/new_compilers/ic2023.2.3/compiler/lib/intel64_lin`
- `-lqkmalloc`

---

**Peak Compiler Invocation**

C benchmarks:
- `icx`

C++ benchmarks:
- `icpx`

Fortran benchmarks:
- `ifx`

---

**Peak Portability Flags**

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64

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Cisco Systems
Cisco UCS X210 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPEC CPU®2017 Integer Rate Result
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Cisco Systems
Cisco UCS X210 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPECrate®2017_int_base = 428
SPECrate®2017_int_peak = 441

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Feb-2024
Tested by: Cisco Systems
Hardware Availability: Feb-2024
Software Availability: Dec-2023

Peak Portability Flags (Continued)

557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -w -std=c11 -m64 -Wl,-z,muldefs
-fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2(pass 1)
-ffast-math -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/home/specdev/new_compilers/ic2023.2.3/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/home/specdev/new_compilers/ic2023.2.3/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2(pass 1)
-ffast-math -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xsapphirerapidps -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -fno-alias
-L/home/specdev/new_compilers/ic2023.2.3/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: basepeak = yes

C++ benchmarks:

520.omnetpp_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

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Cisco Systems
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Peak Optimization Flags (Continued)

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic2023p2-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2023p2-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-EMR-revB.xml