SPEChpc™ 2021 Tiny Result

Lenovo Global Technology
ThinkSystem SR665 V3 (AMD EPYC 9654)

SPEChpc 2021_tny_base = 50.2
SPEChpc 2021_tny_peak = 50.2

-hpc2021 License: 28
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Test Date: Jan-2023
Hardware Availability: Nov-2022
Software Availability: Nov-2022

505.lbm_t
513.soma_t
518.tealeaf_t
519.clvleaf_t
521.miniswp_t
528.pot3d_t
532.sph_exa_t
534.hpgmfv_t
535.weather_t

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Model</th>
<th>Ranks</th>
<th>Thrds/Rnk</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
<td>505.lbm_t</td>
<td>OMP</td>
<td>96</td>
<td>8</td>
<td>33.5</td>
<td>67.2</td>
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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.
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Software Summary

Compiler: Intel oneAPI Compiler 2022.1.0
MPI Library: Intel MPI Library for Linux OS, Build 20220227
Other MPI Info: --
Other Software: --
Base Parallel Model: OMP
Base Ranks Run: 96
Base Threads Run: 8
Peak Parallel Models: OMP
Minimum Peak Ranks: 96
Maximum Peak Ranks: 96
Max. Peak Threads: 8
Min. Peak Threads: 8

Node Description: ThinkSystem SR665 V3

Hardware

Number of nodes: 4
Uses of the node: Compute
Vendor: Lenovo Global Technology
Model: ThinkSystem SR665 V3
CPU Name: AMD EPYC 9654
CPU(s) orderable: 1,2 chips
Chips enabled: 2
Cores enabled: 192
Cores per chip: 96
Threads per core: 2
CPU Characteristics: Max Boost Clock up to 3.7 GHz
CPU MHz: 2400
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 1 MB I+D on chip per core
L3 Cache: 384 MB I+D on chip per chip
32 MB shared / 8 cores
Other Cache: None
Memory: 1536 GB (24 x 64 GB 2Rx4 PC5-4800B-R)
Disk Subsystem: 1x ThinkSystem 2.5" 5300 480GB SSD
Other Hardware: None
Accel Count: --
Accel Model: --
Accel Vendor: --
Accel Type: --
Accel Connection: --
Accel ECC enabled: --
Accel Description: --
Adapter: Nvidia Mellanox ConnectX-6 HDR
Number of Adapters: 1
Slot Type: PCI-Express 4.0 x16
Data Rate: 200 Gb/s
Ports Used: 1

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SPEChpc 2021 Tiny Result

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Node Description: ThinkSystem SR665 V3

Hardware (Continued)
Interconnect Type: ConnectX-6 HDR

Interconnect Description: Nvidia Mellanox ConnectX-6 HDR

Vendor: Nvidia
Model: Nvidia Mellanox ConnectX-6 HDR
Switch Model: QM8700
Number of Switches: 1
Number of Ports: 40
Data Rate: 200 Gb/s
Firmware: 3.9.0606
Topology: Mesh
Primary Use: MPI Traffic, NFS Access

Submit Notes

The config file option 'submit' was used.
submit = mpiexec -hostfile $[top]/4nodes -np ranks -genv OMP_NUM_THREADS=$threads -ppn %{NRNK} $command

Compiler Version Notes

====================================================================================================
 FC  519.clvleaf_t(base) 528.pot3d_t(base) 535.weather_t(base)
====================================================================================================
Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
ifx: command line error: no files specified; for help type "ifx -help"

====================================================================================================
 CC  505.lbm_t(base) 513.soma_t(base) 518.tealeaf_t(base) 521.miniswp_t(base) 534.hpgmgfv_t(base)
====================================================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
clang: warning: -Z-reserved-lib-stdc++: 'linker' input unused
 [-Wunused-command-line-argument]

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Compiler Version Notes (Continued)

==============================================================================
CXXC 532.sph_exa_t (base)
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2022.1.0 Build 20220316
Copyright (C) 1985-2022 Intel Corporation. All rights reserved.
clang: warning: -Z-reserved-lib-stdc++: 'linker' input unused
[-Wunused-command-line-argument]
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
mpiicc -cc=icx

C++ benchmarks:
mpiicpc -cxx=icx

Fortran benchmarks:
mpiifort -fc=ifx

Base Portability Flags

505.lbm_t: -lstdc++
513.soma_t: -lstdc++ -DSPEC_NO_VAR_ARRAY_REDUCE
518.tealeaf_t: -lstdc++
519.clvleaf_t: -lstdc++
521.miniswp_t: -lstdc++
528.pot3d_t: -lstdc++
532.sph_exa_t: -lstdc++
534.hpgmgfv_t: -lstdc++
535.weather_t: -lstdc++

Base Optimization Flags

C benchmarks:
-Ofast -mprefer-vector-width=512 -march=core-avx2 -ipo -fiopenmp
-ansi-alias

C++ benchmarks:
-Ofast -mprefer-vector-width=512 -march=core-avx2 -ipo -fiopenmp

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#### Base Optimization Flags (Continued)

**C++ benchmarks (continued):**
- `-ansi-alias`

**Fortran benchmarks:**
- `-Ofast` `-mprefer-vector-width=512` `-march=core-avx2` `-ipo` `-fiopenmp` `-nostandard-realloc-lhs` `-align array64byte`

#### Base Other Flags

**C benchmarks (except as noted below):**
- `-Ispecmpitime`

521.miniswp_t: `-Ispecmpitime/`

534.hpgmgfv_t: `-Ispecmpitime`

**C++ benchmarks:**
- `-Ispecmpitime`

**Fortran benchmarks:**

519.clvleaf_t: `-Ispecmpitime`

#### Peak Optimization Flags

**C benchmarks:**

505.lbm_t: `basepeak = yes`

513.soma_t: `basepeak = yes`

518.tealeaf_t: `basepeak = yes`

521.miniswp_t: `basepeak = yes`

534.hpgmgfv_t: `basepeak = yes`

**C++ benchmarks:**

532.sph_exa_t: `basepeak = yes`

(Continued on next page)
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Peak Optimization Flags (Continued)

Fortran benchmarks:

519.clvleaf_t:basepeak = yes
528.pot3d_t:basepeak = yes
535.weather_t:basepeak = yes

The flags file that was used to format this result can be browsed at

You can also download the XML flags source by saving the following link:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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