SPEChpc™ 2021 Large Result

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Intel

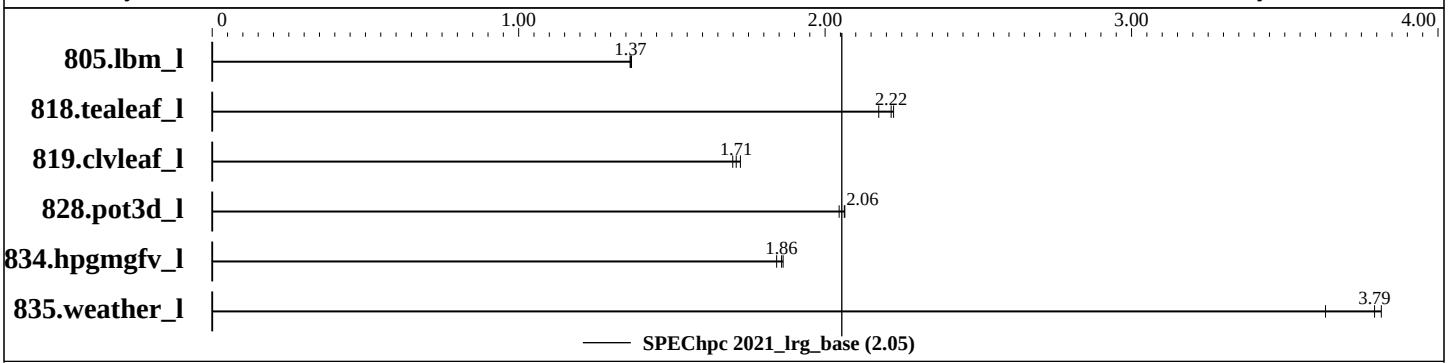
Endeavour: Intel Server D50DNP1SBB (Xeon Max 9480)

SPEChpc 2021_lrg_base = 2.05

SPEChpc 2021_lrg_peak = Not Run

hpc2021 License: 13
Test Sponsor: Intel
Tested by: Intel

Test Date: Jun-2024
Hardware Availability: Jan-2023
Software Availability: Mar-2024



Results Table

Benchmark	Base									Peak								
	Model	Ranks	Thrds/Rnk	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Model	Ranks	Thrds/Rnk	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
805.lbm_l	OMP	512	7	**1996**	**1.37**	1998	1.36	1992	1.37									
818.tealeaf_l	OMP	512	7	**654**	**2.22**	652	2.22	667	2.18									
819.clvleaf_l	OMP	512	7	1236	1.70	**1228**	**1.71**	1218	1.72									
828.pot3d_l	OMP	512	7	**2206**	**2.06**	2204	2.06	2224	2.05									
834.hpgmgfv_l	OMP	512	7	**1803**	**1.86**	1798	1.86	1819	1.84									
835.weather_l	OMP	512	7	898	3.82	943	3.63	**903**	**3.79**									

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

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Hardware Summary

Type of System:	Homogenous Cluster
Compute Node:	Intel Server D50DNP1SBB (Xeon Max 9480)
Interconnect:	Mellanox HDR
Compute Nodes Used:	32
Total Chips:	64
Total Cores:	3584
Total Threads:	7168
Total Memory:	20 TB
Max. Peak Threads:	--

Software Summary

Compiler:	Intel oneAPI Compiler 2024.1.0
MPI Library:	Intel MPI Library 2021.12 for Linux OS
Other MPI Info:	None
Other Software:	None
Base Parallel Model:	OMP
Base Ranks Run:	512
Base Threads Run:	7
Peak Parallel Models:	Not Run
Minimum Peak Ranks:	--
Maximum Peak Ranks:	--
Max. Peak Threads:	--
Min. Peak Threads:	--

Node Description: Intel Server D50DNP1SBB (Xeon Max 9480)

Hardware

Number of nodes:	32
Uses of the node:	Compute
Vendor:	Intel
Model:	Intel Server D50DNP1SBB (Xeon Max 9480)
CPU Name:	Intel Xeon Max 9480
CPU(s) orderable:	1, 2 chips
Chips enabled:	2
Cores enabled:	112
Cores per chip:	56
Threads per core:	2
CPU Characteristics:	Turbo Boost Technology up to 3.5 GHz
CPU MHz:	1900
Primary Cache:	32 KB I + 48 KB D on chip per core
Secondary Cache:	2 MB I+D on chip per core
L3 Cache:	112.5 MB I+D on chip per chip
Other Cache:	None
Memory:	640 GB (16 x 32GB 2Rx8 PC5-4800B-R + 8 x 16GB HBM2 3200 MT/s)
Disk Subsystem:	1 x 1 TB NVMe U.2 2.5" SSD
Other Hardware:	None
Accel Count:	None
Accel Model:	None
Accel Vendor:	None
Accel Type:	None
Accel Connection:	None
Accel ECC enabled:	None
Accel Description:	None
Adapter:	Mellanox ConnectX-6 HDR
Number of Adapters:	1
Slot Type:	PCI-Express 4.0 x16
Data Rate:	200Gbit/s
Ports Used:	1

(Continued on next page)

Software

Accelerator Driver:	None
Adapter:	Mellanox ConnectX-6 HDR
Adapter Driver:	23.04-0.5.3
Adapter Firmware:	20.37.1014
Operating System:	Rocky Linux 8.8 (Green Obsidian) 4.18.0-477.15.1.el8_8.x86_64
Local File System:	xfs
Shared File System:	PANASAS FS
System State:	Run level 5
Other Software:	None

Node Description: Intel Server D50DNP1SBB (Xeon Max 9480)

Hardware (Continued)

Interconnect Type: Mellanox HDR

Interconnect Description: Mellanox HDR

Hardware

Vendor:	Mellanox
Model:	Mellanox HDR
Switch Model:	Mellanox MQM8790-HS2F Quantum HDR InfiniBand Switch
Number of Switches:	18
Number of Ports:	40
Data Rate:	200 Gbit/s
Firmware:	20.36.1010
Topology:	Fat-tree
Primary Use:	MPI Traffic

Software

: --

Submit Notes

```
The config file option 'submit' was used.
```

General Notes

```
The PANASAS filesystem as described on this result page was formerly
generally available.  At the time of this publication, it may
not be shipping, and/or may not be supported, and/or may fail
to meet other tests of General Availability described in the
SPEC HPG Policy document, http://www.spec.org/hpg/policy.html

HBM is configured as HBM cache mode.
```

Compiler Version Notes

```
==============================================================================
 CC  805.lbm_l(base) 818.tealeaf_l(base) 834.hpgmgfv_l(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler 2024.1.0 (2024.1.0.20240308)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir:
  /global/panfs05/admin5/opt/intel/oneAPI/2024.1.0/compiler/2024.1/bin/compiler
Configuration file:
  /global/panfs05/admin5/opt/intel/oneAPI/2024.1.0/compiler/2024.1/bin/compiler/../icx.cfg
```

(Continued on next page)

Compiler Version Notes (Continued)

```
------------------------------------------------------------------------------

==============================================================================
 FC  819.clvleaf_l(base) 828.pot3d_l(base) 835.weather_l(base)
------------------------------------------------------------------------------
ifx (IFX) 2024.1.0 20240308
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------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
`mpiicc -cc=icx`

Fortran benchmarks:
`mpiifort -fc=ifx`

Base Portability Flags

805.lbm_l: `-lstdc++ -std=c++14`
818.tealeaf_l: `-lstdc++ -std=c++14`
834.hpgmgfv_l: `-lstdc++ -std=c++14`

Base Optimization Flags

C benchmarks:
`-O3 -Ofast -xCORE-AVX512 -mprefer-vector-width=512 -qopt-multiple-gather-scatter-by-shuffles -fiopenmp -ffast-math -flto -funroll-loops`

Fortran benchmarks:
`-O3 -Ofast -xCORE-AVX512 -mprefer-vector-width=512 -qopt-multiple-gather-scatter-by-shuffles -fiopenmp -ffast-math -flto -funroll-loops -nostandard-realloc-lhs -align array64byte`

Base Other Flags

C benchmarks:
`-Wno-incompatible-function-pointer-types`

The flags files that were used to format this result can be browsed at

http://www.spec.org/hpc2021/flags/HBM.html
http://www.spec.org/hpc2021/flags/Intel_compiler_flags.2024-12-11.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/hpc2021/flags/HBM.xml
http://www.spec.org/hpc2021/flags/Intel_compiler_flags.2024-12-11.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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